

# ERRATA SHEET

**Date:** 2004 Apr 19  
**Document Release:** Version 1.0  
**Device Affected:** P89LPC925

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2004 Apr 19

**Identification:**

The typical P89LPC925 devices have the following top-side marking:

```
P89LPC925x x
xxxxxxx xx
xxYYWW R
```

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC925:

| Revision Identifier (R) | Comment                 |
|-------------------------|-------------------------|
| 'A'                     | Initial device revision |

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

**Errata Overview - Functional Problems**

| Functional Problem | Short Description                                 | fixed in revision | added |
|--------------------|---|-------------------|-------|
| ADC.1              | Single Step mode multi channel boundary interrupt | none              | v1.0  |
| ADC.2              | Timer/Edge with Scan Mode Counter Reset           | none              | v1.0  |

**Errata Overview - AC/DC Deviations**

| AC/DC Deviation | Short Description | fixed in revision | added |
|-----------------|-------------------|-------------------|-------|
| -               | -                 | -                 | -     |

**Errata Notes**

| Note               | Short Description              | added |
|--------------------|--------------------------------|-------|
| V <sub>DD</sub> .1 | V <sub>DD</sub> Power cycling. | v1.0  |

## Functional Deviations of P89LPC925

### ADC.1: Single Step mode multi channel boundary interrupt

**Introduction:** The ADC on the LPC925 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Single Step mode where the ADC will step through the selected channels on each ADC start condition.

**Problem:** When the ADC is in Single Step mode with more than 1 channel selected, and a boundary interrupt occurs to any of the lower selected channel-bits, a write to the ADMODA register to clear the BNDI bit before all the selected channels are converted will reset the channel selection counter and the ADC will go back and wait at the lowest selected channel for the next conversion. .

**Workarounds:**

- 1) Clear the lower channel bits including the boundary interrupted channel in ADCINS register before the next start request.
- 2) Use the default boundary channel, not clear BNDI bit until all channels are converted.

### ADC.2: Timer/Edge trigger with scan mode

**Introduction:** The ADC on the LPC925 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Timer / Edge trigger mode where the ADC will generate an ADC start condition on the timer or edge on a pin. Scan mode is an ADC feature where the ADC will scan through all selected channels on an ADC start condition.

**Problem:** When the ADC is in Timer or Edge mode, with scan mode, and more than 1 channel is selected, and the repeat conversion on timer or edge is selected, the channel counter increments to last selected channel on first conversion, but on all subsequent conversion triggers the counter is not reset, so only the last channel is converted over and over again.

**Workarounds:**

- 1) To reset the counter that sticks on the last channel the ADC can be disabled and enabled again.
- 2) Switch from ADC mode to DAC mode and back.

## **Electrical and Timing Specification Deviations of P89LPC925**

**No known errata**

## Errata Notes

### **V<sub>DD</sub>.1: V<sub>DD</sub> Power cycling**

To generate a proper Power-On-Reset (POR), V<sub>DD</sub> must have dropped below 0.2V before being powered back up. Power-cycling without V<sub>DD</sub> having dropped below 0.2V may result in incorrect Program Counter values.

Please also see the V<sub>POR</sub> specification in LPC925 Datasheet, DC electrical characteristics. Section 8.15 (Reset) states that during a power cycle, V<sub>DD</sub> must fall below V<sub>POR</sub>.