Product Qualification Package CGD942C

870 MHz, 23 dB Gain power doubler amplifier

Rev. 01 — October 13, 2009

Document information

Info	Content
Keywords	Product Qualification Package
Abstract	This document presents the characteristics of CGD942C power doubler CATV amplifier.

founded by Philips

Revision history

Rev	Date	Description
01	20091013	Initial Release

Contact information

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1. Device description

1.1 Introduction

Hybrid amplifier module in a SOT115J package, operating at a supply voltage of 24 V (DC), employing Hetero Field Effect Transistor (HFET) GaAs dies.

Features:

- High output power capability
- Excellent linearity
- Extremely low noise
- Excellent return loss properties
- Rugged construction
- Unconditionally stable

1.2 Chemical content

For Chemical content information CGD942C (SOT115), please follow link below:

http://www.nxp.com/search/chemical_content/

1.3 Mounting & soldering recommendations for CATV products

1.3.1 Mounting Recommendations

The heat sink mounting surface must be flat, free of burrs and oxidation and parallel to the mounting surface. The heat sink, mounting base and ground leads should be properly RF-grounded. Heat sink compound should be applied sparingly and evenly on the mounting base. When mounting CATV hybrid modules, the UNC screws must first be turned finger- tight. The screws should then be tightened to within the tolerance of 0.5 Nm minimum and 0.7 Nm maximum.

1.3.2 Soldering Recommendations

Leads may be plugged-in onto the corresponding sockets or soldered directly into the circuit for robustness and for better RF-connection. The latter is specifically recommended for products that use Sn-plated leads. Soldering may be done using soldering iron with a maximum temperature of 260 ºC for not more than 3 seconds with a minimum lead length between the closest solder joints and the module of 3 mm.

1.3.3 General information

Table 1. Product

NXP Type	Device Type description	Package	Status	Order / 12NC
CGD942C	870 MHz, 23dB Gain GaAs power doubler	SOT115J	Released	9340 595 07112

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Table 2. Manufacturing locations

Sub assembly	Final Assembly & test
NXP Semiconductors (APK) *	NXP Semiconductors (APP3)*

* Certified ISO 14001 & ISO 9001

Table 3. Package Technology

Package SOT115J	
Package Outline	- rectangular single-ended package - aluminium flange - 2 vertical mounting holes - 2 ´ 6-32 UNC and 2 extra horizontal mounting holes - 7 gold-plated in-line leads

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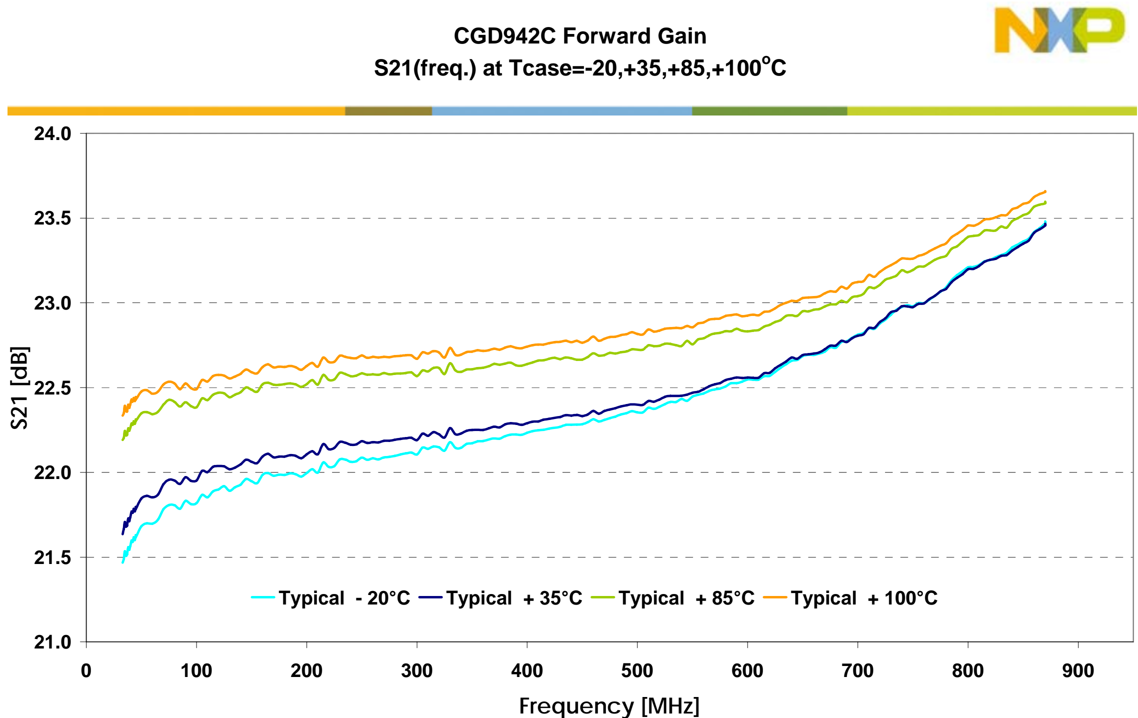
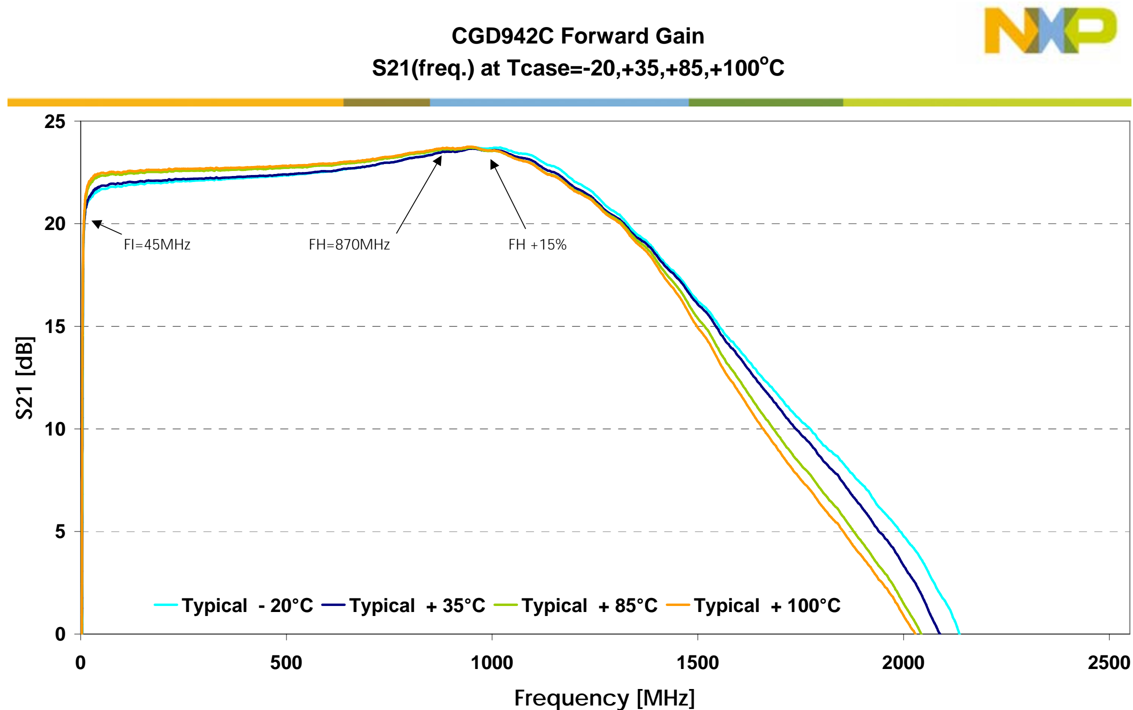
2. Characterization data

2.1 S-parameters and stability





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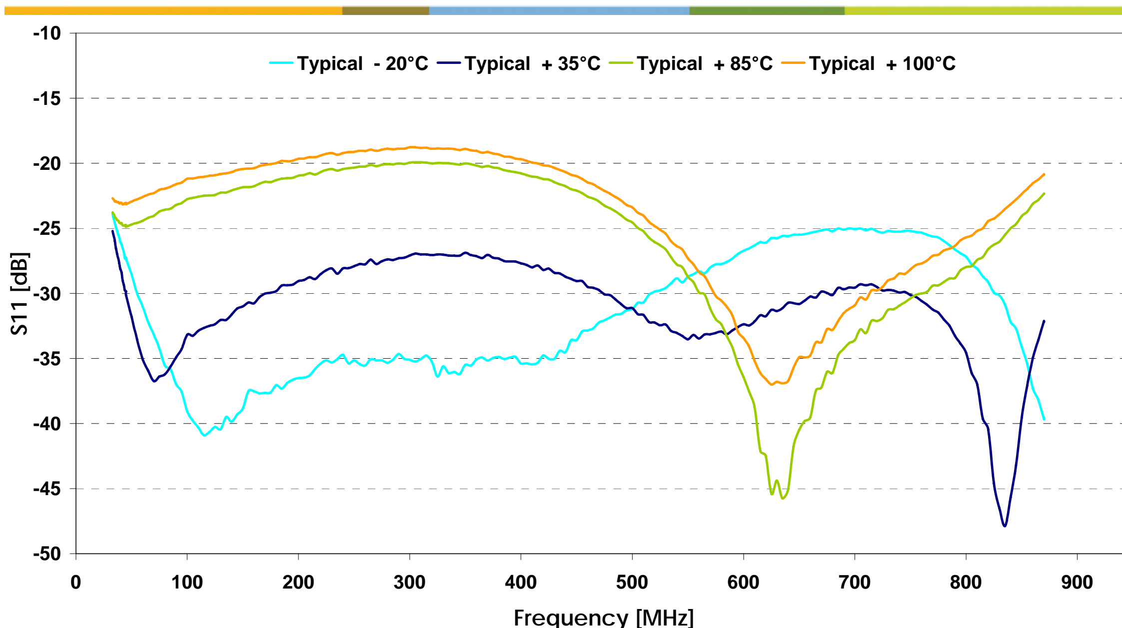

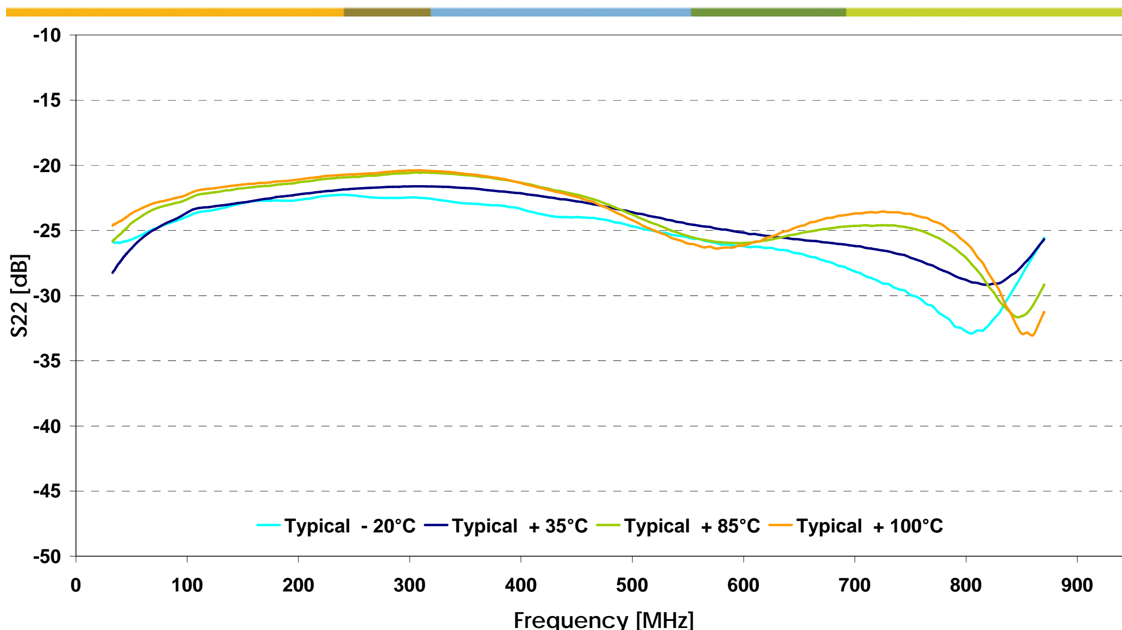

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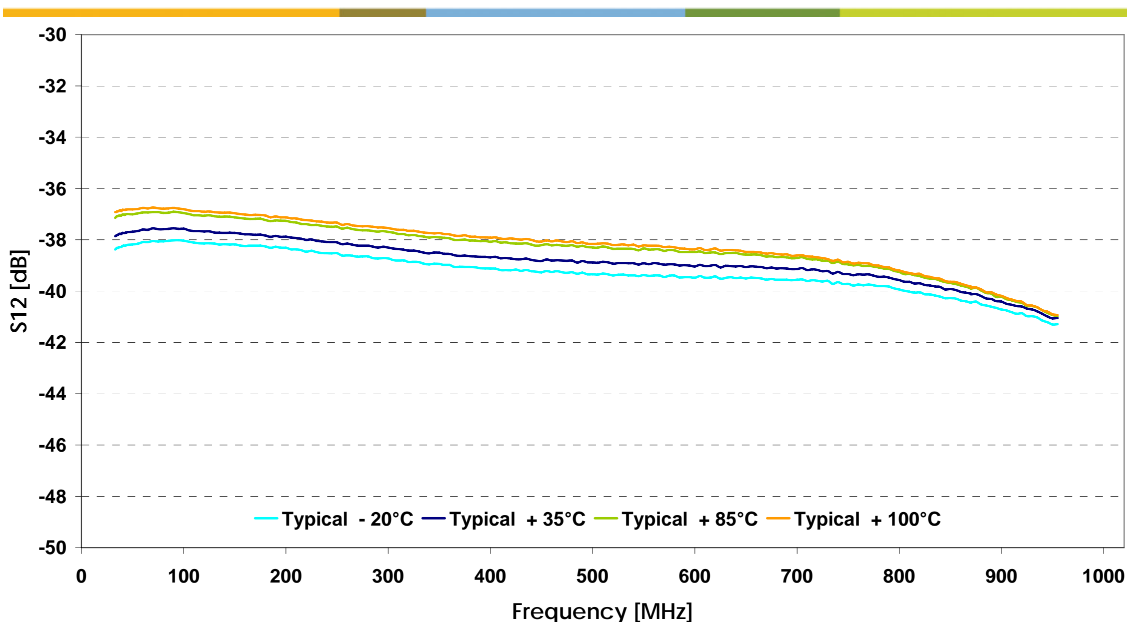

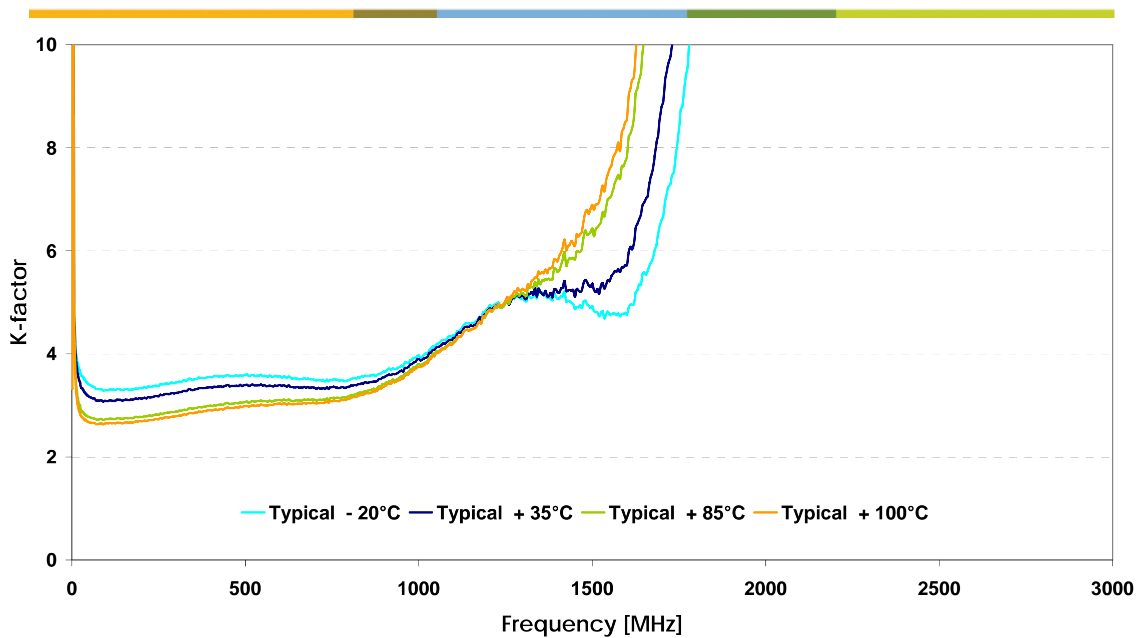

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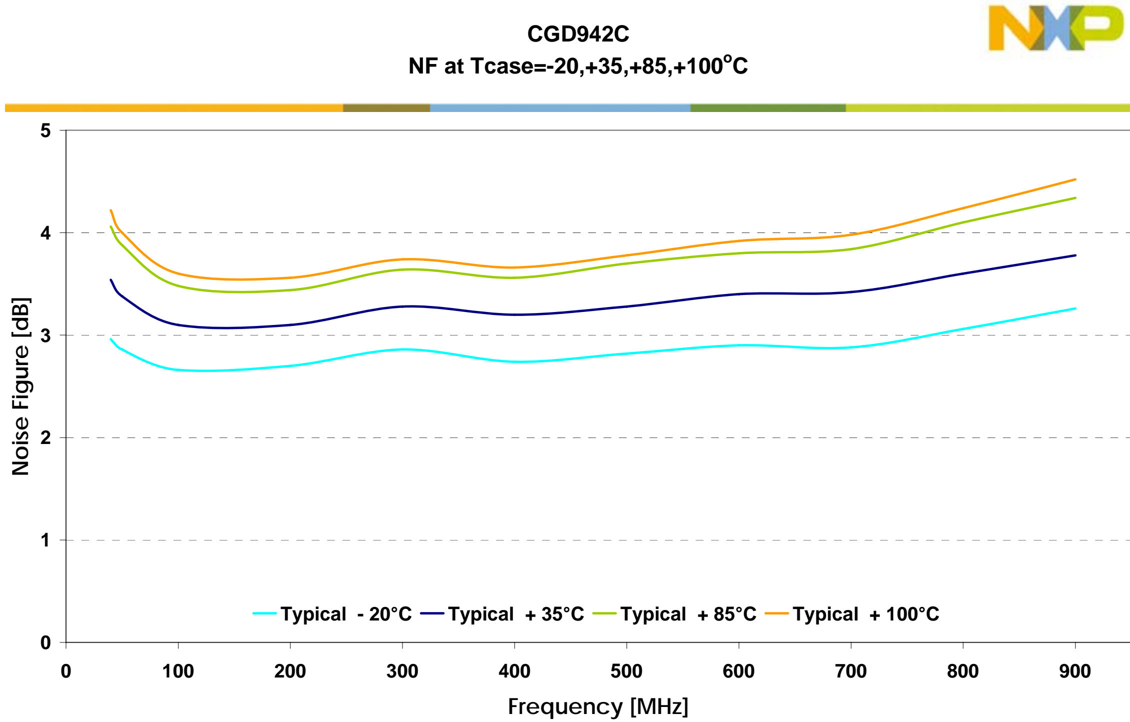
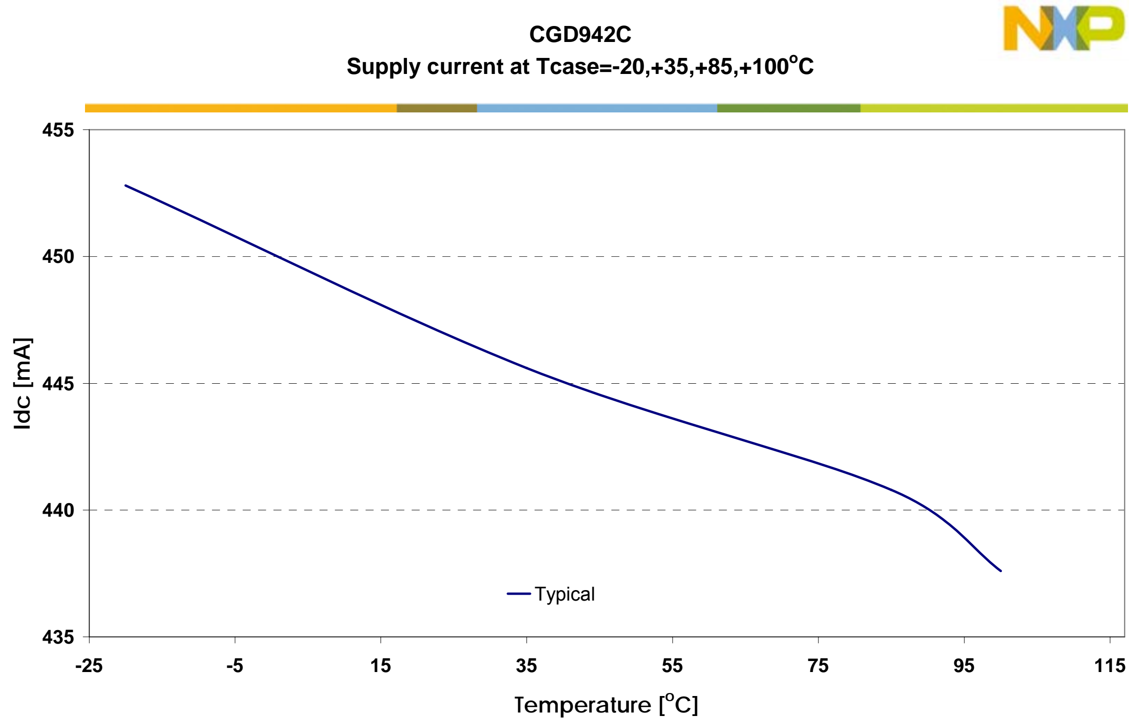
2.2 Noise



2.3 Supply current



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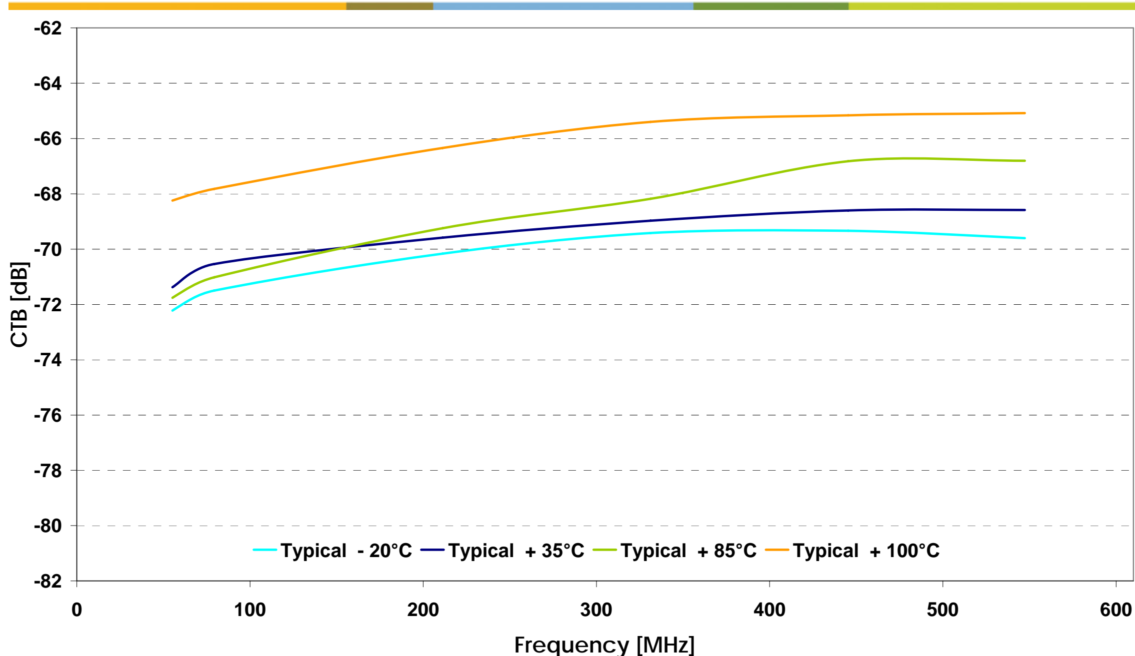
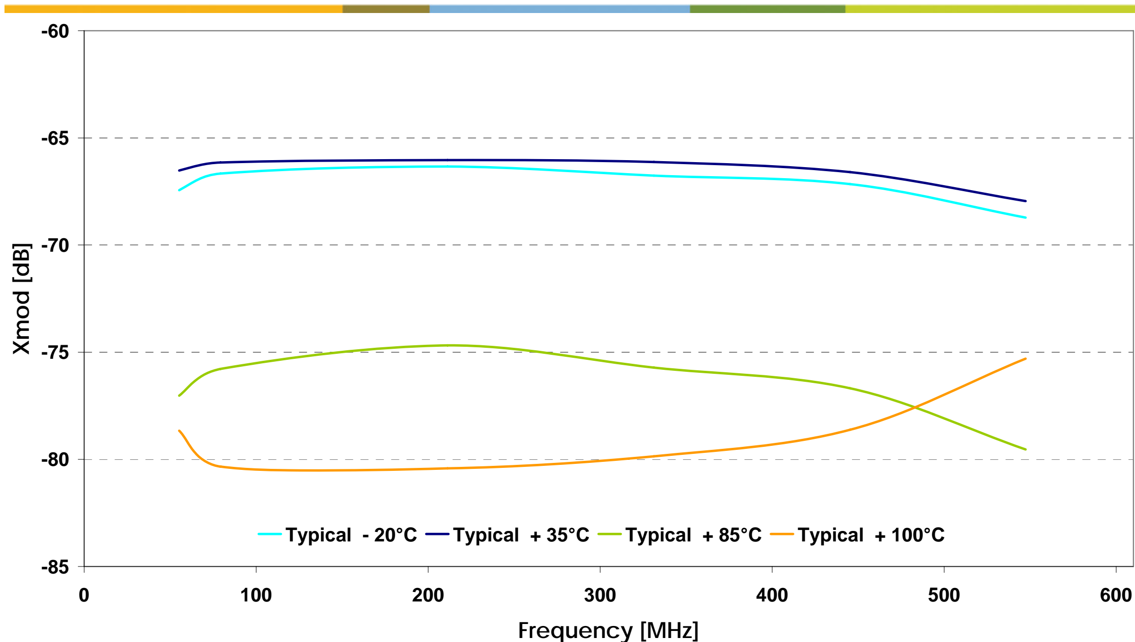
2.4 Distortion





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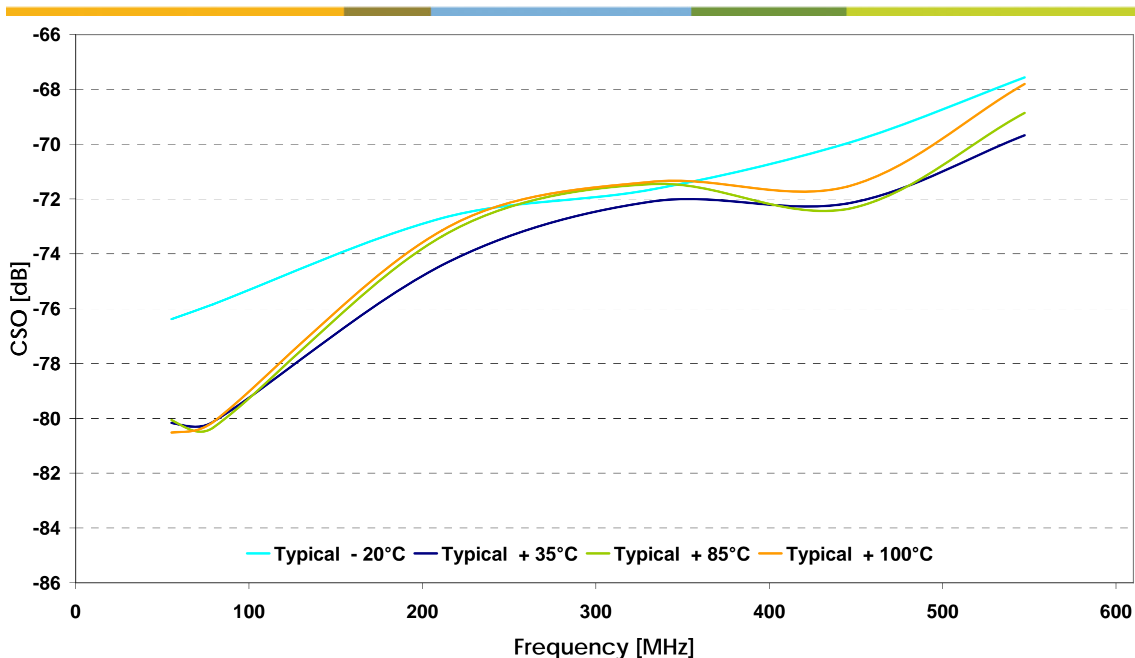

2.5 Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R_{th} (j-mb)	Thermal resistance from junction to mounting base	T_{mb} = 100°C $+V_B$ = 24V I_{tot} = 445mA	6.4	K/W

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3. Reliability results

3.1 Environmental test results

NXP endurance tests are based on JEDEC and IEC standards.
Reliability testing applies the basic principle of structural similarity.

Table 5. Environmental test overview

Test	Test Conditions	End point measurement	Sample size	Sample	Result
High Temperature Operating Life (HTOL) JESD22-A 108-B	T_{mb} = 125°C, V_{B+} = 27V	1000 hrs	60	Structural similar to CGD944C, CGD1044 and CGD1044Hi	**PASS**
Temperature Humidity No Bias (THNB) JESD 22 A110-B	T_a = 85°C / RH = 85%	1000 hrs	20	Structural similar to CGD944C, CGD1044 and CGD1044Hi	**PASS**
Temperature Cycling (TMCL) JESD22-A104	T_a = -40°C to +125°C	150 cycles	105	Structural similar to CGD944C, CGD1044 and CGD1044Hi	**PASS**
Drop test (DT) JESD22-B104 / B110 / B111	H = 1m	-	6	Structural similar to CGD1042	**PASS**
Highly Accelerated Stress Test (HAST) JESD 22 A110-B	T_a = 130°C / RH =85%, V_{B+} = 24V	96 hrs	80	Sub-package (HVQFN)	**PASS**
High Temperature Storage Life (HTSL) JESD22-A103	T_a = 175°C	1000 hrs	150	Sub package (HVQFN)	**PASS**
Temperature Cycling (TMCL) JESD22-A104	T_a = -65°C to +150°C	200 cycles	230	Sub package (HVQFN)	**PASS**

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Table 6. Assessed Early Failure Rate

Life Test	Conditions	Early Failure Rate
HTOL	Confidence level: 60% T_{junc} ref: 55°C Sample size: 83	11036 FPM

Table 7. Assessed Intrinsic Failure Rate

Life Test	Conditions	Intrinsic Failure Rate
HTOL	Confidence level: 60% T_{junc} ref: 55°C Activation Energy: 1.5eV Acceleration factor determined according Arrhenius formula	6 FIT

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3.2 Electrical Overstress

Table 8. Electrical Overstress results

Test	Test Conditions	Pass / Level
ESD (HBM)	Per JEDEC: JESD22-A114	**2000V**
ESD (Bias)	Per IEC61000-4-2	**700V**
Surge pulse	Per IEC 1000-4-5: $+V_B$ = 40V RF-in = 80V RF-out = 80V T_{mb} = 35°C	**PASS**
RF overload	$V_{i\,(RF)}$ = 75 dBmV, single tone * Z_L = 0 - ∞ Ω T_{mb} = 35°C Full recovery after 1 hour under bias condition * At the most critical frequency within the operational pass band	**PASS**
DC supply over-voltage	Duration = 1 min. T_{mb} = 35°C	**48V**
Transient on top of DC supply	$+V_B$ = 24V T_{mb} = 35°C Pulse width / frequency = 0.1ms/1500Hz 1.0ms/150Hz 10.0ms/15Hz 100.0ms/1.5Hz Number of pulses = 20	**30V**

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4. ESD precaution

Introduction

This document is designed to help you gain a better understanding of semiconductor devices, so as to ensure the quality and reliability of the devices that you incorporate into your designs.

Electrostatic charge generation

In neutral material, the net charge of protons (positive charge) and electrons (negative charge) is zero. When the surface of one material is rubbed along that of another, local (frictional) heating can transfer energy to the electrons near the surface in excess of the Coulomb binding energy. Such electrons may leave their outer valence orbit and be trapped in an outer valence orbit in the other material. Thus two ions will be formed: 1) positive, for electron-donor material and 2) negative, for electron-acceptor material. Friction between any two surfaces involving at least one non-conductive material is a potential generator of electrostatic (triboelectric) charge; the magnitude and polarity of the charge depends on; the materials involved. Charge magnitude and polarity depends on the sum of the separations from the neutral boundary of the two materials in the triboelectric series (Table 1) frictional heat, which depends on speed and applied force surface conductivity. Part of the charge may be drained off during and after rubbing, inhibiting build up of maximum possible voltage, but this is true only for surface conductivities below 10E9 per Surface Square.

A grounded operator cannot drain charge from a non-conductive object. Thus, an operator's clothing may be charged even though a conductive wrist strap grounds his body. Similarly, charged plastic boxes or trays will not be discharged by a grounded operator or bench top.

Induction

Static charges can be transferred by induction; that is, without direct contact. Objects that can transfer charges by induction include the plastic boxes, trays and covers used extensively in production lines. An ESD-sensitive device charged by induction can be damaged if touched by a grounded operator. Removing static charges from insulating materials can only be achieved by use of ionizers.

ESD precautions

In the following section are some hints to avoid ESD damage.

For more detailed information see JEDEC standard JESD625-A, which establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD).

The ESD workstation

Essential features of a workstation for handling ESD devices are shown in Fig. 1. Adaptations for inspection, assembly, repair and other purposes should respect these guidelines:

- Conductive work-surface sheet resistance 10 K Ω to 1 M Ω per square meter
- Resistor for grounding wrist strap between 0.9M Ω and 5M Ω.
  Maximum ground current 2 mA: enough for operator to feel a fault but well below danger level
- All test equipment grounded
- Switching transients suppressed

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– All metal table trim, support frames and brackets grounded
– Cotton working garments
– Static-safe rails, bags, foam pads and shorting clips available, if needed.

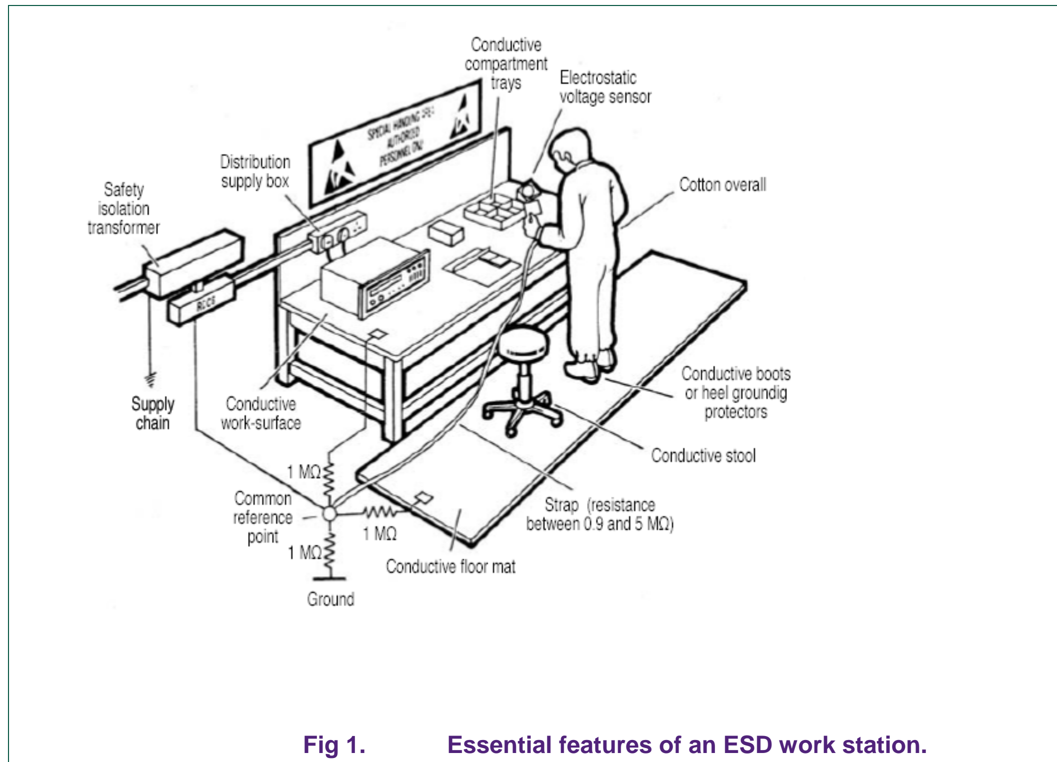

Fig 1. Essential features of an ESD work station.

4.1 Circuit layout precautions

Designing of a circuit board for ESD-sensitive devices should allow for handling by persons unaware of the ESD hazard. Observe the following precautions:

– Tracks to and from ESD-sensitive devices should not pass board edges, to minimize the risk of their being touched in handling.
– Where possible, connect a resistor of about 1 M Ω between conductors from ESD-sensitive devices and board inputs and outputs.
– Avoid long signal lines; they increase the risk of induced large-signal pick-up.
– Observe the maximum rated values for supply turn-on and turn-off transients. Suppress power supply turn-on and turn-off transients, power supply ripple or regulation and ground noise, to avoid exceeding the Absolute Maximum ratings. Fast zener protection diodes are useful here.
– Label the board with an ESD warning.
– Make sure that the service documentation calls attention to the use of ESD-sensitive devices and the precautions to be taken with them.

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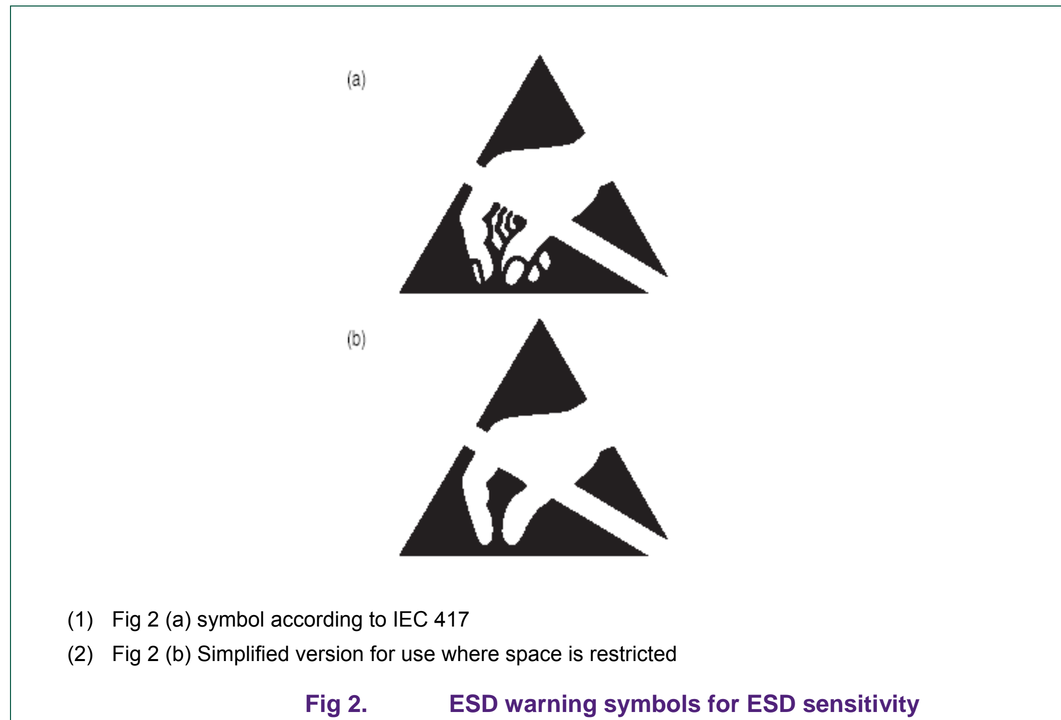
Marking of ESD-sensitive devices

IEC 417 and MIL-STD-1686 recommend that the symbol shown in Fig. 2(a) is used to mark ESD sensitive devices. The symbol should be supplemented by the notice 'ATTENTION – observe precautions for handling ELECTROSTATIC SENSITIVE DEVICES'. Where space is restricted, the simplified symbol shown in Fig. 2(b) may be used. Symbol and lettering should be in black on a yellow ground.



(1) Fig 2 (a) symbol according to IEC 417

(2) Fig 2 (b) Simplified version for use where space is restricted

Fig 2. ESD warning symbols for ESD sensitivity

User precautions

As a general rule, ESD-sensitive devices should always be handled at an ESD station conforming to Fig. 1. Pay particular attention to stores and inspection areas where personnel may not be fully aware of ESD hazards.

Packing and storage

ESD-sensitive devices are packed in antistatic or conductive boxes or rails. Intimate (tube, tape, bag etc.) and proximity (level 1 box) packing is marked with the Fig. 2 symbol. ESD-sensitive devices not supplied in antistatic packing should be returned to the supplier. ESD-sensitive devices should be stored in their original packing, preferably in a cool place set aside for the purpose. Do not unpack them until they are required for incoming inspection or use in production.

Receiving inspection

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Do not put ESD-sensitive devices where static discharges can occur, even if they have protective packing. In their immediate vicinity avoid the presence of:

- Materials which can develop static charges (see Fig. 3)
- Electrical switching equipment and tools.

These precautions also apply to assemblies that incorporate ESD-sensitive devices.

Unpack and handle the devices at an ESD workstation generally conforming to Fig. 1. Take care that the devices are not exposed to the voltage pulses that can occur when switching the power supply on and off. Increase the supply voltage slowly to its normal value before applying test signals, to avoid the latching effect that occurs when the signal voltage exceeds the supply voltage. During testing, and especially when going from one test to another, ensure that all supplied voltages are under control. If possible, ground all unused inputs during tests. Do not allow a signal to remain on an input when the power supply is switched off. If necessary, connect a buffer stage between the signal source and the input in such a way that it automatically switches off the signal when the power supply is switched off.

After testing, repack the devices in their original anti-static packing; keeping the warning label intact. Repack at an ESD workstation.

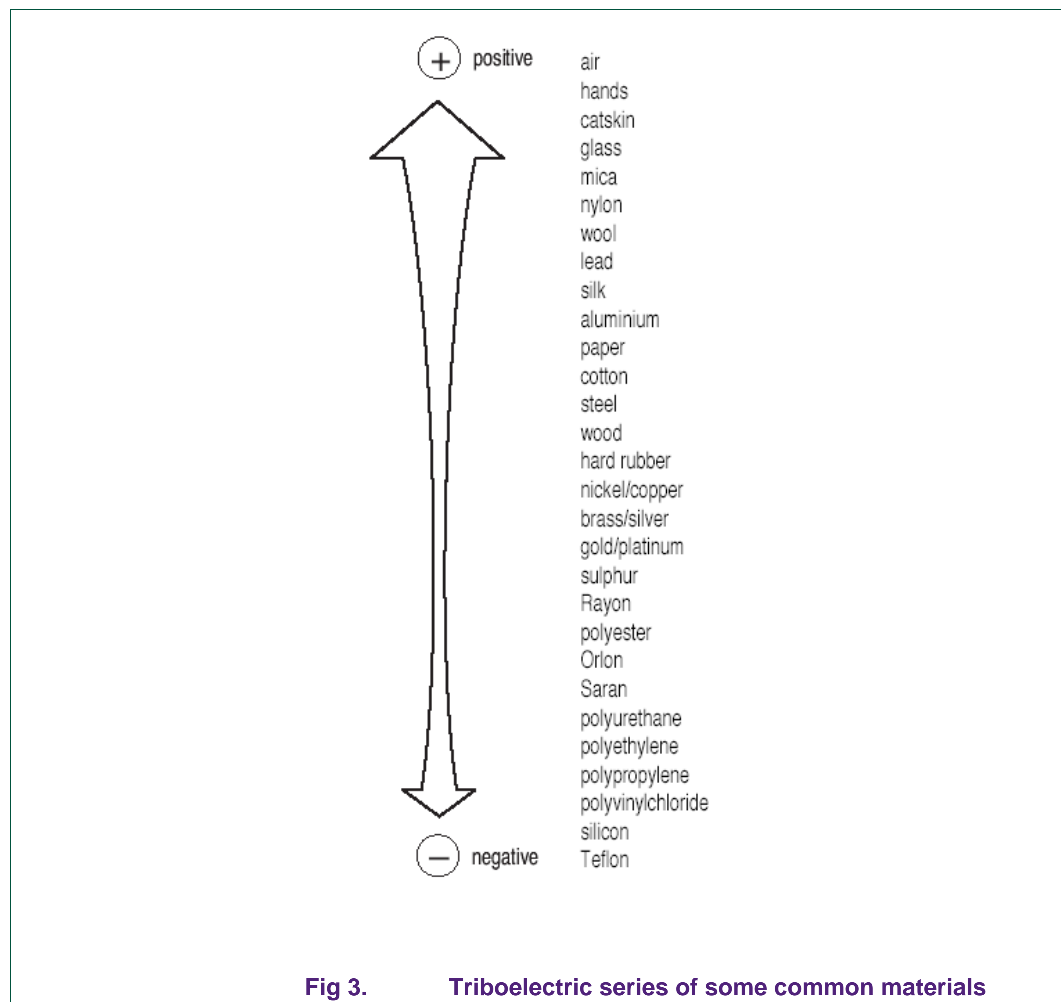

Fig 3. Triboelectric series of some common materials

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Assembly precautions

ESD-sensitive devices should be the last components to be inserted in a circuit board or system.

Manual insertion: Use an ESD workstation.

Automatic insertion: Ground insertion equipment and machinery. Use only tools of conductive or antistatic material.

Use grounded component tongs to remove ESD sensitive devices from their antistatic packing. Do not remove more components at a time than are immediately required.

Ground the soldering iron or bath. Do not solder to circuits that are connected to a switched-on power supply. Ensure that every work surface on which a circuit board may be placed is provided with a conductive or anti-static sheet big enough to receive the whole board.

Handle boards that contain ESD-sensitive devices as single components. Pack them in antistatic or conductive packing. Label them with an ESD warning. Ground all handling personnel.

Measurement precautions

Place the board, soldered side down, on a conductive or antistatic foam pad to discharge any static electricity. Remove short-circuit clips. Handle the board only by its edges, remove it from the foam pad for testing. After testing, replace it on the foam pad for transport.

Repair and maintenance precautions

Switch off the equipment in which the board is incorporated before removing a board containing ESD-sensitive devices. For repair and maintenance use an ESD workstation arranged as shown in Fig. 1. Place the board on an antistatic foam pad. Observing the 'Assembly precautions', remove and replace the faulty device. After testing, replace the board in the equipment.

Static detection and prevention equipment

A wide range of commercial products is available to help detect static electricity, equip workstations and prevent ESD. They range from conductive bags, gloves, mats, foam, wrist straps and boxes, through to static voltmeters, ionizers and ESD simulators. Careful use of available products can help locate and prevent ESD hazards, and so improve quality wherever semiconductors are.

Limitations of anti-static agents

Anti-static agents – conductive sprays – are commonly used to protect against ESD. Although they do protect against charging by friction, they do not form an effective shield and therefore give no protection against charge induction. The only sure protection against charge induction is a Faraday cage shielding the protected object from all possible sources of induced charge.

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