Alpha run on SnPb and Sn plated SMD components

A verification of Sn plated component for a low temperature reflow profile

CTB594-02-2270 2002-07-25

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Electronic Packaging & Assembly

ING. J.M. SCHEER

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Abstract

An alpha-run was carried out to demonstrate that a lead-free finish (Sn-plating) can also be used in standard reflow processes were temperatures are below the melting point of the Sn finish. No soldering defects were observed for a total of 30.000 components (90.000 soldered joint) with Sn finish. An equal amount of SnPb plated components was also assembled to function as a reference.

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Published by: **Philips Electronics Nederland B.V.**
Philips Centre for Industrial Technology
Eindhoven, The Netherlands

Title: Alpha run on SnPb and Sn plated SMD components, A verification of Sn plated component for a low temperature reflow profile
Author: Ing. J.M. Scheer
Document code: CTB594-02-2270
Date: 2002-07-25
Distribution:
Status: Released

If you have any comment to make, please feel free to contact the author:

Philips CFT
Electronic Packaging & Assembly
Ing. J.M. Scheer
PO Box 218 / SFK-028
5600 MD Eindhoven Tel.: (+31 40 27)36907
The Netherlands Fax: (+31 40 27)36815

Copies of this document can be ordered from the distributor:

Philips CFT
CFT Electronic Packaging & Assembly
Ing. J.M. Scheer
PO Box 218 / SFK-028
5600 MD Eindhoven Tel.: (+31 40 27) 36907
The Netherlands Fax: (+31 40 27) 36815

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1 Introduction

For Discrete Semiconductors General Applications Hamburg an α-verification was carried out on Sn plated (lead-free) components in a standard reflow process. The minimum temperature as specified for current reflow processes is 210°C.
Although the melting point of Sn is 232°C, feasibility of this type of plating was already proven as part of the activities concerning the introduction of lead free soldering.
For the α-verification SMD components with Sn and SnPb plating were used.

An α-verification, or assembly trial, is the next step after feasibility is proven and consists of a large-scale assembly test to determine a ppm level that can be expected in a production environment. Therefore it is required to use industrial equipment and processes.

2 Materials

2.1 Components

Two types of components were used, SOT346 (SC-59) and SOT490 (SC-89) respectively. Two types of plating were applied on these components: SnPb and Sn for standard (lead-containing) and lead-free type of assembly respectively. From each type of component a total of 15.000 were assembled.
The components were received from GA Hamburg, coded for the type of plating that was applied. Approximately 16.000 components per variation were received.
The appropriate solder land layouts for the board design were taken from Philips Semiconductors layout specifications and can be found in Appendix II.

2.2 Substrates

The applied substrates were standard FR4 PCB's with a thickness of 1.6mm measuring 150 by 200 mm. Cu was present on one side as well as a solder resist mask. The solder lands were plated with Ni and electroless Au. The board layouts can be found in Appendix I.

Incoming inspection consisted of a reflow- or wettability-test and measurements of the dimensions of the solder lands. Figure 1 and Figure 2 show the typical wetting behaviour for the two types of solder land as was observed.

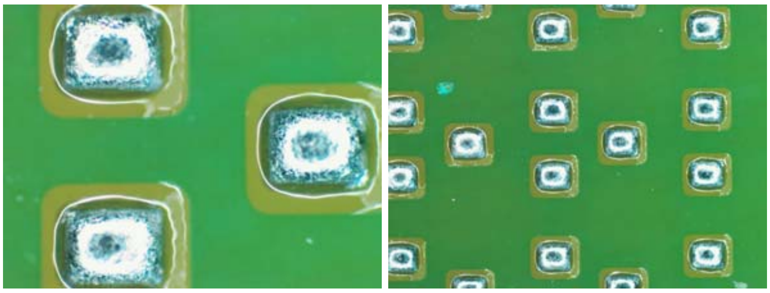

Figure 1 Solder wetting on SOT490 solder lands

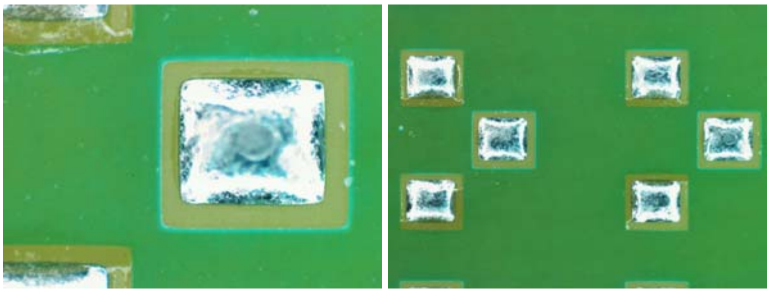

Figure 2 Solder wetting on SOT346 solder lands

Good wetting was observed for the entire board.
Table 1 shows the results from measurements of the dimensions of the two types solder lands.

Table 1 Measurement solder land dimensions

Pad#	**SOT 346**		**SOT490**	
	l	***b***	***l***	***b***
	[µm]	*[µm]*	*[µm]*	*[µm]*
1	739	643	532	439
2	734	644	533	444
3	740	633	536	439
4	736	641	539	441
5	735	637	537	444
6	738	633	535	444
7	734	637	531	437
8	738	637	530	443
9	744	646	535	438
10	739	640	534	436
Average	**738**	**639**	**534**	**441**
StDev	**3**	**4**	**3**	**3**
Spec.	***800***	***700***	***600***	***500***

Upper Spec.	865	755	645	535
Lower Spec.	705	615	525	435

The lower and upper spec limits were calculated using guidelines from the UAN-D1837/020 Miniaturisation Assembly Process Platform (MAPP), which states that the actual values must be within: Design value – 15µm ±10% of the design value.
The measured solder land dimensions are, although a bit low, within specifications, as can be seen in Table 1.

A total of 30 boards were assembled, which results in 60.000 placed components
.

3 Assembly Process

For assembly a production line was used with a DEK stencil printer, an Assembleon FCM 'chip shooter' (using 16 placement heads) and a Vitronics reflow oven with 8 zones. Peak reflow temperature was adjusted such that a temperature of 210°C was measured at the top of the components.
Before assembly all boards were numbered from 050702-01 to 050702-30 (date and serial number). They were processed in ascending order.

3.1 SOLDER PASTE PRINTING

Standard 'No-clean' Solder paste for reflow (AlphaMetals LR735R, PbSn) was used on a laser-cut stencil with a thickness of 150µm. Apertures were 100µm smaller than the copper defined solder lands. The stencil was cleaned after every 10 print cycles.
For printing a metal squeegee was used with the following (relevant) process settings:

- Print speed: 50 mm/s
- Squeegee Pressure: 6 kg
- Release speed: 1 mm/s

The release speed was chosen such that the screen was released gently from the board. Due to the large amount of paste this value was very low compared to standard process settings (5 to 10 mm/s).

For every printed board the solder paste deposits were inspected for presence and shape. *No defects were observed.*

3.2 COMPONENT PLACEMENT

For the FCM a placement program was made based on the board design and image data for the specific components used. The available number of reels enabled the use of all sixteen placement heads. Thus a placement speed of approximately 50.000 components per hour could be realised when fully loaded. A total of 11 boards can then be processed simultaneously.
Placement accuracy of the FCM is 100µm at 3 sigma, which is sufficient for the applied components.
Prior to placement in solder paste a test run was performed were the components were placed on double-sided tape. Inspection of placement accuracy led to a few offsets in order to achieve the required placement accuracy. Criterion here was that the leads of the components must be placed such that they did not exceed the edges of the solder lands.

After placement the boards were inspected for presence and correct alignment of the components. *No defects were found with the exception* *of a single upside-down placed component, most likely due to a tape and reel error.*

3.3 Reflow

A reflow profile was created to ensure a maximum component temperature of 210°C in the reflow zone.
4 thermocouples were used to measure the board and component temperature at two positions (centre and edge).
A fifth thermocouple was used to measure the actual air temperature in the different zones. Figure 3 shows the measured temperature profiles.

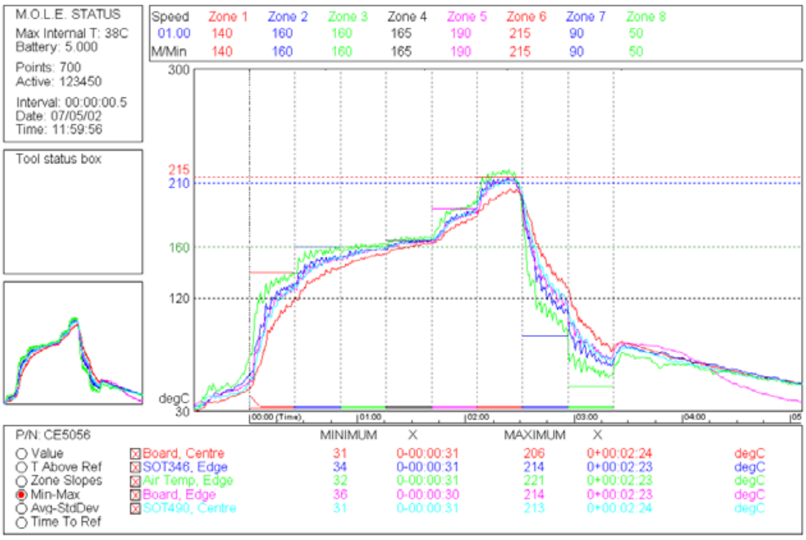

Figure 3 Reflow profile as measured

From this profile it is clear that the maximum temperature that was measured was 214°C for the components, however, the actual temperature was approximately 4°C lower. This was confirmed during a calibration step of the thermocouples were upward deviations from 3 to 4 degrees at room temperature were found.
The measured board temperature was lower compared to the component temperature, which is due to the larger area that needs to be heated.
The applied profile includes a temperature equalisation zone, which is common in the industry to decrease temperature differences between components with different dimensions and/or specific heat. Such a profile sets higher demands to the flux in the solder paste, thus a worst-case scenario was simulated. The duration of the entire profile was 4 minutes and 20 seconds.
Figure 4 shows how and where the thermocouples were applied.

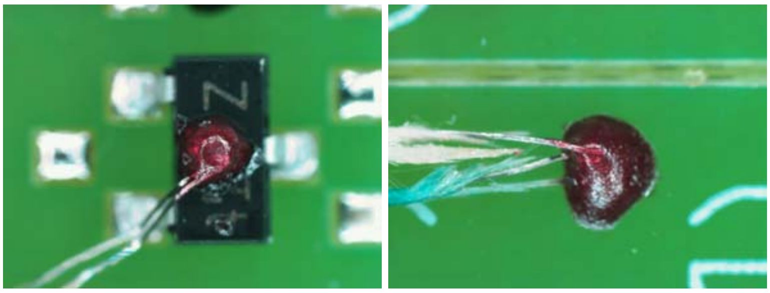

Figure 4 Thermocouples on component and board

SMD adhesive (red) was used to fixate the thermocouples to the components and board respectively.

After reflow the boards were visually inspected for defects as poor wetting or solder balling, none were found.

4 Inspection

A complete visual inspection was done after assembly and reflow using a Leica Stereo microscope with a magnification factor of 6.5 or higher. The soldered joints were inspected under an angle of approximately 45°. Inspection concentrated on the appearance of the soldered joints and any indications that wetting was not optimal.
No defects were found.

With a statistical program the following ppm levels can then be calculated (95% reliability).

Table 2 PPM levels for component and plating type (component and soldered joint level)

Comp.	***Plating***	***Number***	***Defects***	***ppm Lower Level***	***ppm Upper Level***
Component Level					
SOT346	Sn	15.000	0	0	200
SOT346	SnPb	15.000	0	0	200
SOT490	Sn	15.000	0	0	200
SOT490	SnPb	15.000	0	0	200
Soldered joints Level					
SOT346	Sn	45.000	0	0	67
SOT346	SnPb	45.000	0	0	67
SOT490	Sn	45.000	0	0	67
SOT490	SnPb	45.000	0	0	67

Figure 5 shows the two types of components and plating at an angle.

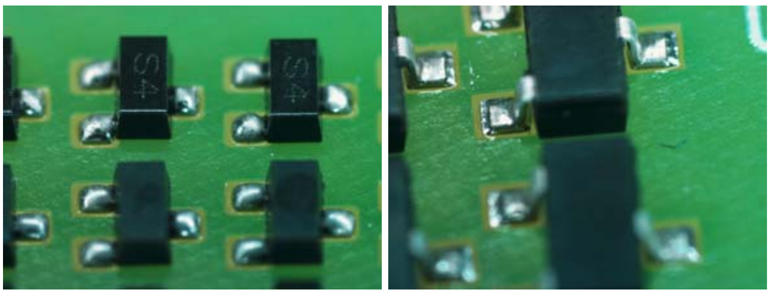

Figure 5 SOT490 & 346 (left & right) SnPb & Sn plated (top & bottom row)

Figure 6 shows the soldered joints of Sn and SnPb plated leads (SOT490), left and right respectively.

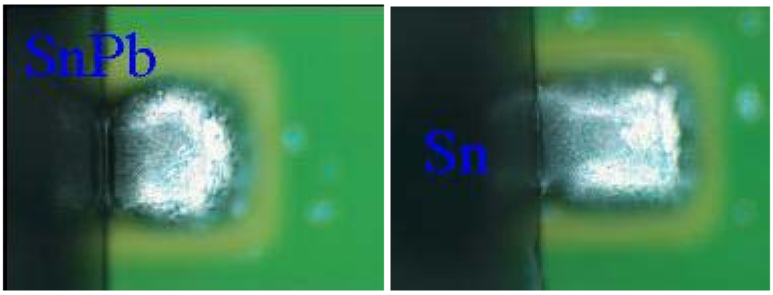

Figure 6 Detail of soldered joints of SOT490

It is visible that the shape of the soldered joint with the Sn plated leads is slightly different compared to the SnPb plated lead. The wetting however is good.
Figure 7 shows the typical soldered joints of the SOT346 components. Differences in plating were not visible here.

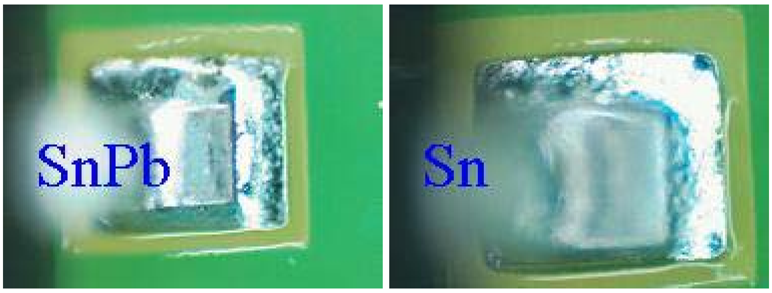

Figure 7 Detail of soldered joints SOT346

A spare board that was available was used to make cross-sections of the soldered joints.

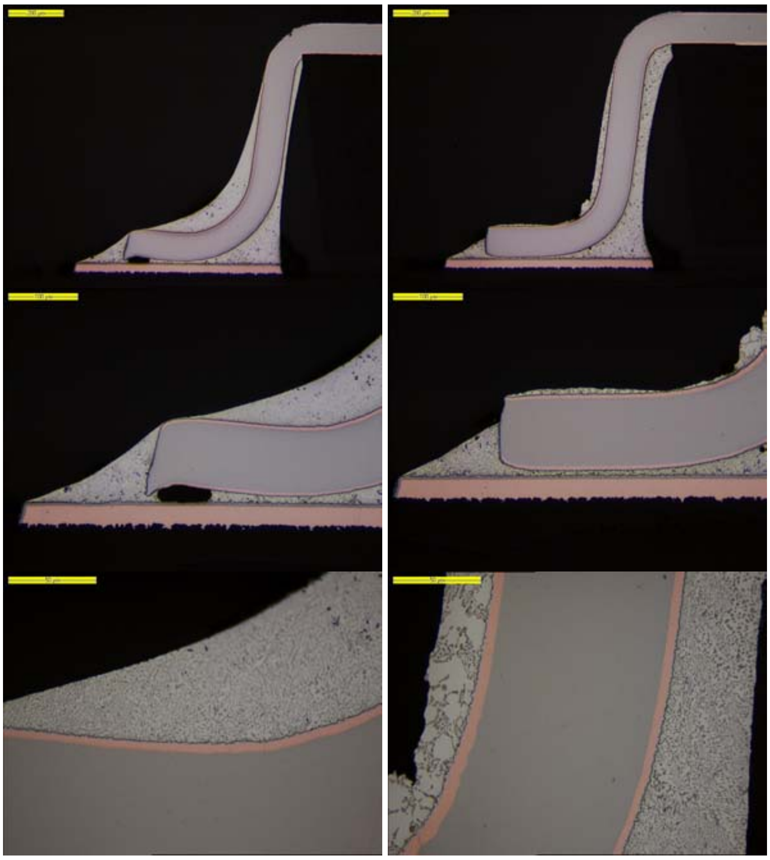

Figure 8 Sn and SnPb plated leads (left and right respectively)

From these images it is clear that a good wetting occurred. Variances in wetting behaviour can be deduced to surface effects as oxidation and/or damage inflicted by bending of the leads.

5 Conclusion

The initial goal to prove the feasibility of using lead-free lead finishes as Sn plating in a ‘normal’ lead containing reflow profile was met. Reflow behaviour of Sn plated components is comparable to PbSn plated components, also when subjected to a minimum low temperature reflow profile (T_{min} =210°C).
Minor differences in appearance of the soldered were observed for the SOT490 with the smallest leads. However, this did not result in wetting defects.
Apparently the Sn finish, that has its melting point at 232°C, easily forms an intermetallic joint with the SnPb based solder at a temperature as low as 210°C. This mechanism is reliable enough to ensure good wetting behaviour for large numbers of soldered joints.
For all Sn plated components that were assembled 0 defects were found on 90.000 inspected soldered joints. Statistical analysis with 95% confidence predicts a defect level less than 25 ppm (soldered joint level).

Appendix I, Board Layout

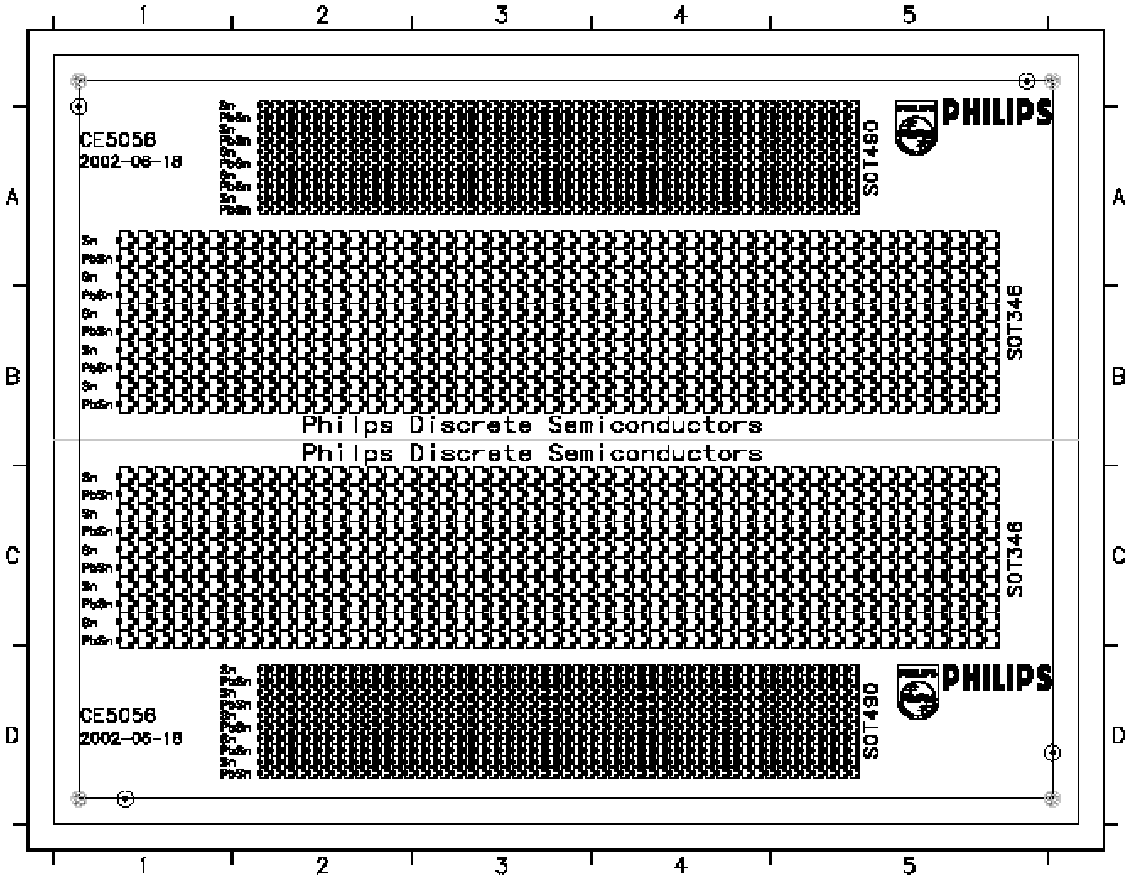

Figure 9 Board Layout, Components.

Appendix II, Footprint layouts

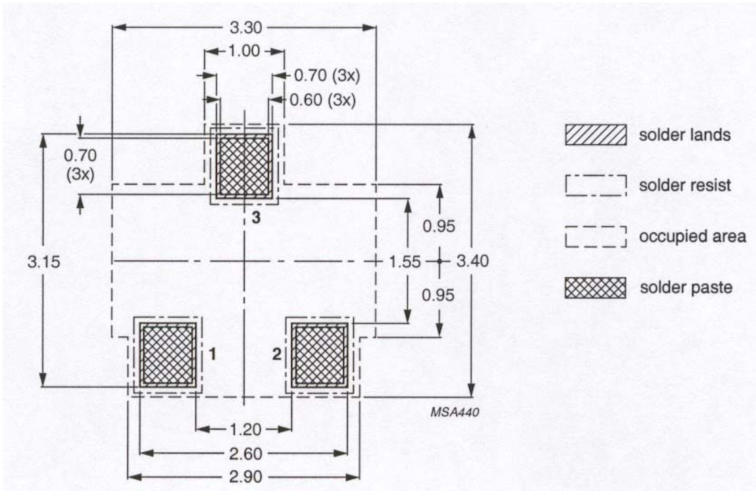

Figure 10 Footprint for SOT346 (SC-59) component (reflow)

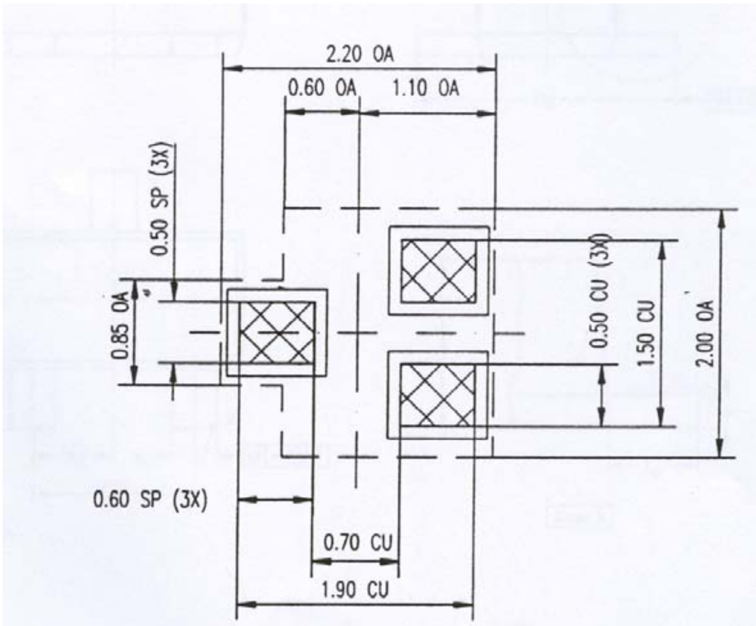

Figure 11 Footprint for SOT490 (SC-89) component (reflow)