MF1 IC S50 05

Bumped sawn wafer on UV-tape addendum

Rev. 3.2 — 4 April 2007
102032

Product data sheet
PUBLIC

1. General description

The MF1 ICS 50 05 is a contactless smart card IC designed for card IC coils following the mifare card IC coil design guide and is qualified to work properly in NXP reader environment, which is built according to NXP specification.

This specification describes electrical, physical and dimensional properties of sawn bumped wafers on UV-tape.

2. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Ordering Code
MF1ICS5005W/V1D		Die on bumped sawn wafer	9352 774 55005

3. Mechanical specification

3.1 Wafer

- Diameter: 8”
- Thickness: 150 µm ± 15 µm
- Flatness: not applicable
- PGDW: 24892

3.2 Wafer backside

- Material: Si
- Treatment: ground and stress relieve
- Roughness: R_a max. 0.5 µm,

  R_t max. 5 µm

3.3 Chip dimensions

- Chip size: 1.11 x 1.06 mm
- Scribe lines: x-line: 91.2 µm

  y-line: 91.2 µm

founded by Philips

3.4 Passivation

- Type: sandwich structure
- Material: PSG / Nitride(on top)
- Thickness: 500 nm / 600 nm

3.5 Au bump

- Bump material: > 99.9% pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 µm
- Bump height uniformity:
  - within a die: ± 2 µm
  - within a wafer: ± 3 µm
  - wafer to wafer: ± 4 µm
- Bump flatness: ± 1.5 µm
- Bump size:
  - LA, LB, VSS [1] 104 x 104 µm
  - TESTIO[1] 89 x 104 µm
- Bump size variation: ± 5 µm
- Under bump metallization: sputtered TiW

3.6 Fail die identification

All fail dies are inked according to electrical test results and additionally the results of mechanical / visual inspection.

Electronic wafer mapping covers the electrical test results and additionally the results of mechanical / visual inspection.

Remark: Substrate is connected to VSS.

1.Pads VSS and TESTIO are disconnected when wafer is sawn.

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4. Limiting values

Table 2. Limiting values[1][2][3]

In accordance with the Absolute Maximum Rating System (IEC 134)

Symbol	Parameter		Min	Max	Unit
I_{IN}	Input Current		-	30	mA
P_{tot}	Total power dissipation per package		-	200	mW
T_{STOR}	Storage temperature range		-55	+125	°C
T_{OP}	Operating temperature		-25	70	°C
V_{ESD}	Electrostatic discharge voltage	[4]	2	-	kV
I_{LU}	Latch-up current		± 100		mA

[1] Stresses above one or more of the limiting values may cause permanent damage to the device

[2] These are stress ratings only. Operation of the device at these or any other conditions above those given in the characteristics section of the specification is not implied

[3] Exposure to limiting values for extended periods may affect device reliability

[4] MIL Standard 883-C method 3015; Human body model: C = 100 pF, R = 1.5 kW

5. Characteristics

5.1 AC Characteristics

Table 3. Characteristics [1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IN}	Input frequency		-	13.56	-	MHz
C_{IN}	Input capacitance (LCR meter HP4258)	22 °C, Cp-D, 13.56 MHz, 2 V	14.4	16.1	17.4	pF
t_W	EEPROM write time		-	2.9	-	ms
t_{RET}	EEPROM data retention		10			years
N_{WE}	EEPROM write endurance		10^5			cycles

[1] Stresses above one or more of the limiting values may cause permanent damage to the device

[2] These are stress ratings only. Operation of the device at these or any other conditions above those given in the characteristics section of the specification is not implied

[3] Exposure to limiting values for extended periods may affect device reliability

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6. Chip orientation and bond pad locations

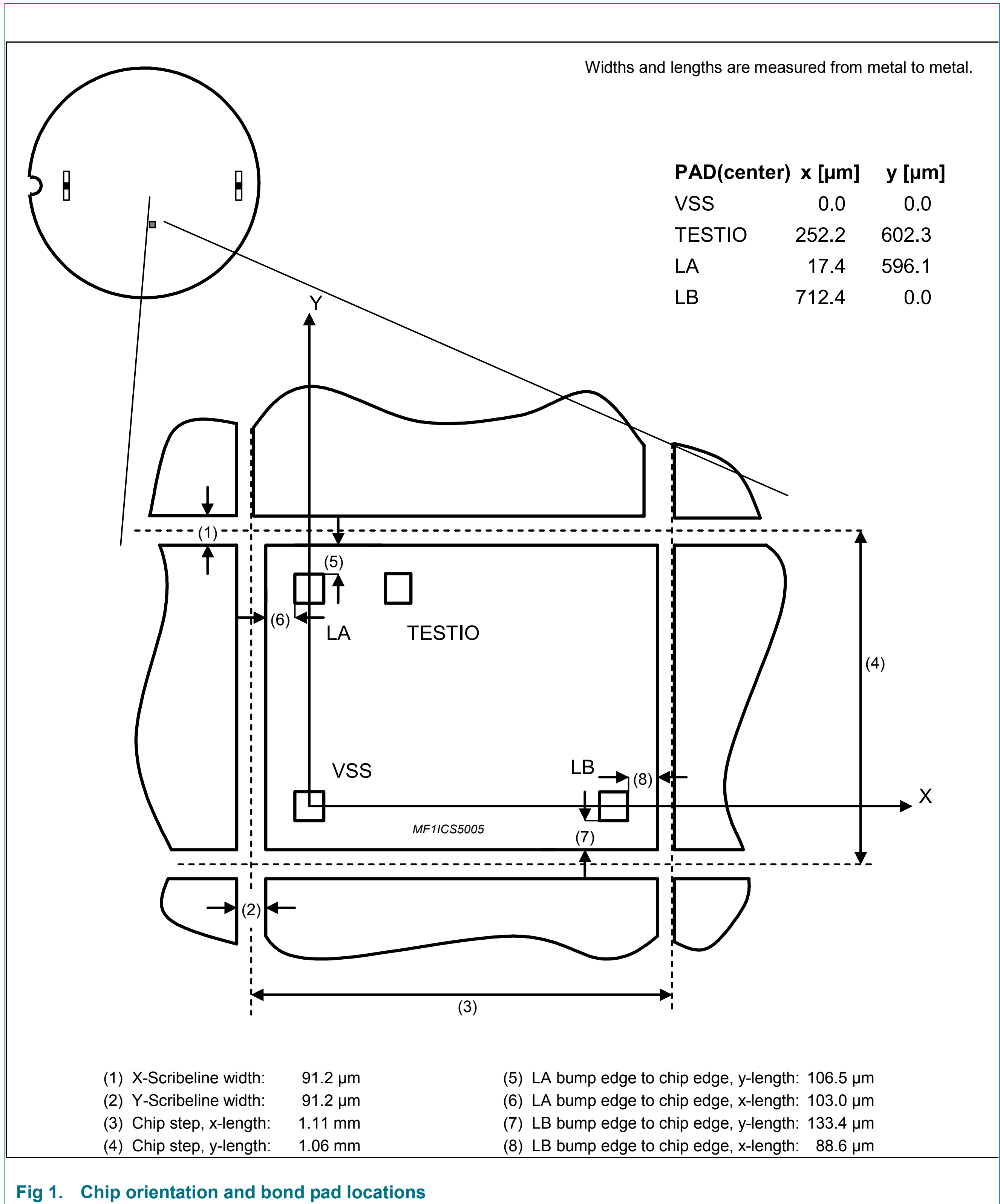

Fig 1. Chip orientation and bond pad locations

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7. References

- data sheet “general wafer specification for 8” wafers on uv-tape”
- data sheet “au bumps layout rules and specification”
- data sheet “standard 4kbyte card ic mf1 ic s70 functional specification”
- product qualification package “standard card ic mf1 ic s70 01”
- application note “mifare, card ic coil design guide”

8. Revision history

Table 4. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
	January 2007	Product data sheet		
102032	4 April 2007	Product data sheet	treatment information	Revision 3.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name.			

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9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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