A Comprehensive Bipolar Avalanche Multiplication Compact Model for Circuit Simulation

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Abstract

In this paper a new comprehensive avalanche multiplication model is presented that takes into account the finite thickness of the epilayer, modulation of the electric field by the collector current (Kirk effect), current spreading in the epilayer and quasi-saturation. Two parameters are needed to model the collector voltage dependency at small current levels and one parameter to describe high current effects. The dependency of the collector-emitter breakdown voltage $BV_{\rm ceo}$ with collector current is shown. The model will be part of the bipolar compact transistor model Mextram 504, but also can be used separately.

1 Introduction

In a bipolar transistor near the breakdown voltage avalanche currents are generated in the base-collector depletion layer. For advanced high-frequency transistors the breakdown voltage is low and avalanche currents are already generated below the supply voltage. This significantly increases the output conductance at high base input impedance. Therefore in circuit design accurate simulation of these effects is essential.

In Ref. [1] a physics based avalanche model is presented that describes the generation of avalanche current as a function of collector voltage. It is well known that the collector current modulates the maximum electric field in the b-c depletion layer. Therefore avalanche multiplication depends besides the collector voltage, also on the collector current. Such a current dependency was already discussed in [1], where the conclusion was that the model can only be used for relative low current densities. In this paper we will extend this avalanche model to include the collector current dependence of the avalanche current, especially for high current densities.

2 Model derivation

The generation of avalanche current is based on Chynoweth's emperical law for the ionization coefficient [2]

$$P_n = \alpha_n \exp\left(\frac{-b_n}{|E|}\right), \tag{1}$$

where α_n is the avalanche coefficient and b_n a critical electric field. We use for an NPN transistor $\alpha_n = 7.05 \cdot 10^7\,\mathrm{m}^{-1}$ and $b_n = 1.23 \cdot 10^8\,\mathrm{V/m}$ and for a PNP transistor $\alpha_p = 1.58 \cdot 10^8\,\mathrm{m}^{-1}$ and $b_p = 2.04 \cdot 10^8\,\mathrm{V/m}$. Because only weak avalanche multiplication is considered the generated avalanche current $I_{\rm avl}$ is proportional to the current $I_{\rm epi}$ passing through the collector epilayer:

$$I_{\rm avl} = I_{\rm epi} \int_{x=0}^{x=W_d} \alpha_n \exp\left(\frac{-b_n}{|E(x)|}\right) \mathrm{d}x. \tag{2}$$

Here W_d is the width of the depletion layer.

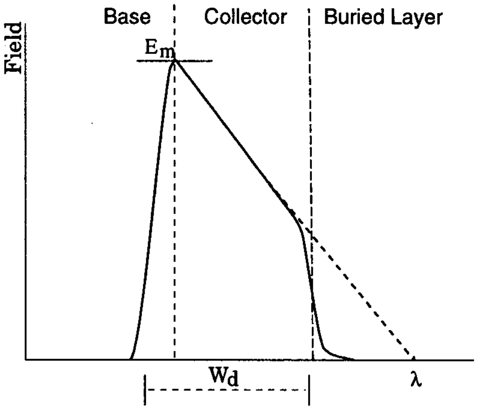

Figure 1: *Schematic electric field distribution. The extrapolation of the electric field becomes zero at the point* λ.

To calculate the avalanche current we have to evaluate the integral of Eq. (2) in the space charge region. This integral is mainly determined by the maximum of the electric field. We make a suitable approximation (fig. 1) around the maximum electric field

$$E(x) = E_m \left(1 - \frac{x}{\lambda}\right) \simeq \frac{E_m}{1 + x/\lambda}, \tag{3}$$

where λ is the point where the extrapolated electric field is zero. Then the generated avalanche current becomes

$$\frac{I_{\rm avl}}{I_{\rm epi}} = \frac{\alpha_n}{b_n} E_m \lambda \left\{ \exp\left(\frac{-b_n}{E_m}\right) - \exp\left(\frac{-b_n}{E_m}\left[1 + \frac{W_d}{\lambda}\right]\right)\right\} \tag{4}$$

The maximum electric field E_m, the depletion layer thickness W_d and the intersection point λ are all dependent on collector voltage and current.

2.1 One dimensional model

First we will define E_m, W_d and λ without taking into account current speading (1-D current flow) and quasi-saturation (no injection region at b-c junction). In contrast to Ref. [1] we will not make use of the b-c capacitance model to calculate W_d. The reason is that the capacitance parameters, and in particular the grading coefficent m_c, are mainly determined by

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the extrinsic b-c capacitance. The avalanche current however is generated in the intrinsic collector region underneath the emitter. We therefore chose a simplified model for the intrinsic base-collector capacitance, only to be used for the avalanche current. We relate E_m, W_d and λ directly to an effective doping level N_{epi} and thickness W_{epi} of the epilayer. These two quantities will be the low current parameters of our model.

For a one sided abrupt b-c junction with $I_{\mathrm{epi}} < I_{\mathrm{hc}} = q\,N_{\mathrm{epi}}\,v_{\mathrm{sat}}\,A_{\mathrm{em}}$ the depletion layer thickness x_d is

$$x_d = \sqrt{\frac{2\,\epsilon}{q\,N_{\mathrm{epi}}}\,\frac{V_{\mathrm{dc}}+V_{\mathrm{cb}}}{1-I_{\mathrm{epi}}/I_{\mathrm{hc}}}}, \qquad I_{\mathrm{epi}} < I_{\mathrm{hc}}, \tag{5}$$

where V_{dc} is the b-c diffusion voltage. The real depletion thickness W_d cannot exceed the epilayer thickness W_{epi}. A smooth and soft transition from x_d to W_{epi} is

$$W_d = \begin{cases} \dfrac{x_d\,W_{\mathrm{epi}}}{\sqrt{x_d^2+W_{\mathrm{epi}}^2}}, & \text{for } I_{\mathrm{epi}} < I_{\mathrm{hc}}, \\ W_{\mathrm{epi}}, & \text{for } I_{\mathrm{epi}} \geq I_{\mathrm{hc}}\,. \end{cases} \tag{6}$$

Here we also included the case $I_{\mathrm{epi}} > I_{\mathrm{hc}}$, when the complete epilayer is depleted.

The average electric field E_{av}, the field at the b-c junction E_0 and the field at the buried layer E_w are

$$\begin{aligned} E_{\mathrm{av}} &= \frac{V_{\mathrm{dc}}+V_{\mathrm{cb}}}{W_d}, & \Delta E &= \frac{q\,N_{\mathrm{epi}}}{2\,\epsilon}\,W_d\left(1-\frac{I_{\mathrm{epi}}}{I_{\mathrm{hc}}}\right), \\ E_0 &= E_{\mathrm{av}}+\Delta E, & E_w &= E_{\mathrm{av}}-\Delta E. \end{aligned} \tag{7}$$

The maximum electric field is either at the base-collector junction (when $I_{\mathrm{epi}} < I_{\mathrm{hc}}$) or at the buried layer (when $I_{\mathrm{epi}} > I_{\mathrm{hc}}$). A transition between the two is given by

$$E_m = \frac{1}{2}\left(E_0+E_w+\sqrt{(E_0-E_w)^2+K}\right), \tag{8}$$

$$K = 0.1\,E_{\mathrm{av}}^2\,\frac{I_{\mathrm{epi}}}{I_{\mathrm{hc}}+I_{\mathrm{epi}}}. \tag{9}$$

Finally we calculate the distance λ between the point where the field is maximal and the point where the extrapolated field is zero:

$$\lambda = \frac{E_m\,W_d}{2\,(E_m-E_{\mathrm{av}})}. \tag{10}$$

For an advanced double-poly process Ref. [3] we show in Fig. 2 the measured and simulated base current versus V_{cb}, for $V_{\mathrm{be}} = 0.75\,\mathrm{V}$. The base current I_b is the forward base current, which is almost constant, minus the avalanche current I_{avl}. Since the collector current density is low ($I_{\mathrm{epi}} \ll I_{\mathrm{hc}}$) it will not modulate the electric field in the depletion layer. In this example mainly the depletion layer thickness determines the collector voltage where I_b starts to decrease. The curvature of I_b is also determined by the (effective) doping level N_{epi}. The agreement between the measured and simulated data is excellent over a large range of collector voltages.

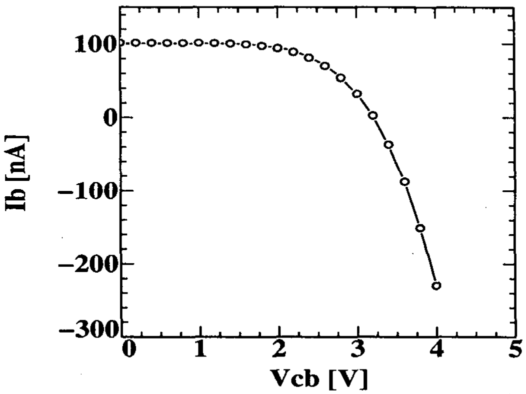

Figure 2: *Measured and simulated base current at small current density $I_{\mathrm{epi}}/I_{\mathrm{hc}}$. The extracted parameters are:* $W_{\mathrm{epi}} = 0.27\,\mu\mathrm{m}$, $N_{\mathrm{epi}} = 1.28\cdot10^{16}\,\mathrm{cm}^{-3}$.

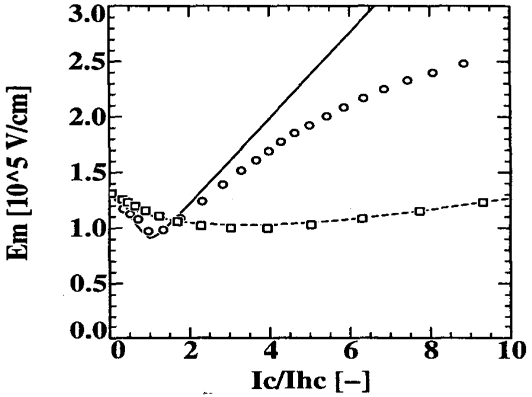

Figure 3: *The maximum electric field E_m as a function of the collector current.* $V_{\mathrm{cb}} = 3.4\,\mathrm{V}$, $W_{\mathrm{epi}} = 0.5\,\mu\mathrm{m}$, $N_{\mathrm{epi}} = 1.0\cdot10^{16}\,\mathrm{cm}^{-1}$. *The emitter width is* $0.5\,\mu\mathrm{m}$. *Circles: 1-D device simulation, squares: 2-D device simulation, solid line: 1-D model, dashed line: 2-D model with S_g* $= 2.6$.

2.2 Current dependency of E_m

The dependency of I_{avl} on collector current is more complicated. In figure 3 we show 1-D and 2-D device simulations of the maximum electric field for a transistor with $W_{\mathrm{epi}} \approx 0.5\,\mu\mathrm{m}$ and $N_{\mathrm{epi}} = 1.0\cdot10^{16}\,\mathrm{cm}^{-3}$. The emitter width is $0.5\,\mu\mathrm{m}$. The circles are the maximum electric field from 1-D device simulation and the solid line is the 1-D compact model. The initial decrease of E_m with collector current is well described by the model. However, for increasing collector current the deviations become larger. The main reason is that now the whole epilayer is depleted and the precise doping profile of both the base and the buried layer become important. The deviation between the 1-D model discussed above and the 2-D device simulation is even larger. Note that already the initial decrease of E_m is modified. We will now discuss this in more detail.

The collector current dependency is complicated due to current spreading in the epilayer and the influence of the steepness of the doping profile of the buried layer. With increasing collector current the maximum electric field moves gradually from the internal b-c junction to the buried layer.

Also in lateral direction E_m becomes position dependent. Near the buried layer the field is maximal at the center of the emitter and decreases toward the sidewall of the emitter. As a consequence the part of the collector current flowing through the center of the emitter sees a higher electric field than the outer part. Because the transistor is now operating at high currents and high voltages also self-heating becomes important.

It is difficult to create a simple geometrical and physics based compact model that describes accurately the avalanche current including all these effects. Therefore we propose a simple model for the behaviour of the maximal electric field E_m as function of the collector current. First the current dependence of the depletion layer thickness x_d is modified by replacing $I_{\mathrm{epi}}/I_{\mathrm{hc}}$ by $I_{\mathrm{epi}}/(I_{\mathrm{hc}}+I_{\mathrm{epi}})$. This leads to

$$x_d = \sqrt{\frac{2\,\epsilon}{q\,N_{\mathrm{epi}}}\,\frac{V_{\mathrm{dc}}+V_{\mathrm{cb}}}{I_{\mathrm{hc}}/(I_{\mathrm{hc}}+I_{\mathrm{epi}})}}. \tag{11}$$

In this way the argument of the square root is always positive. The exact value of x_d when I_{epi} approaches or exceeds I_{hc} is not so important because the maximum of the depletion layer thickness W_d is W_{epi} (see Eq. (6), (12)).

At high collector current the transistor may operate in quasi-saturation. Due to the Kirk effect the internal b-c junction voltage is then forward biased whereas externally it is reverse biased. The effective width to sustain the collector voltage decreases due to the presence of an injection layer with thickness x_i at the internal b-c junction [5]. To avoid that $W_{\mathrm{epi}}-x_i$ gives numerical problems when x_i approaches W_{epi} we replace it by $W_{\mathrm{epi}}\ [1-x_i/(2\,W_{\mathrm{epi}})]^2$. The effective width of the depletion region W_d then is

$$W_d = \frac{x_d\,W_{\mathrm{eff}}}{\sqrt{x_d^2+W_{\mathrm{eff}}^2}}, \qquad W_{\mathrm{eff}} = W_{\mathrm{epi}}\left(1-\frac{x_i}{2\,W_{\mathrm{epi}}}\right)^2. \tag{12}$$

The electric field at the internal b-c junction E_0 is modified in the same way as x_d in Eq. (11)

$$E_0 = \frac{V_{\mathrm{dc}}+V_{\mathrm{cb}}}{W_d} + \frac{q\,N_{\mathrm{epi}}}{2\,\epsilon}\,W_d\left(\frac{I_{\mathrm{hc}}}{I_{\mathrm{hc}}+I_{\mathrm{epi}}}\right). \tag{13}$$

Note that now E_0 is always larger than the average field in the space charge region. To describe the electric field at the buried layer we introduce a spreading parameter S_g, and write

$$\begin{aligned} E_w &= \frac{V_{\mathrm{dc}}+V_{\mathrm{cb}}}{W_d} - \frac{q\,N_{\mathrm{epi}}}{2\,\epsilon}\,W_d\left(S_1-\frac{I_{\mathrm{epi}}}{S_2\,I_{\mathrm{hc}}}\right), && (14)\\ S_1 &= \frac{1+S_g}{1+2\,S_g}, && (15)\\ S_2 &= 1+2\,S_g\left(1+2\,\frac{x_i}{W_{\mathrm{epi}}}\right). && (16) \end{aligned}$$

When $S_g=0$ we regain the 1-D model for E_w. We leave the definitions of E_m and λ unchanged. The avalanche generation current is still given by Eq. (4). In figure 3 we plotted E_m for $S_g=2.6$. The maximum electric field of the 2-D compact model compares reasonably well with the 2-D device simulations.

All the modifications given in this section do not change the V_{cb} dependence of E_m, and hence the avalanche current, at small current densities ($I_{\mathrm{epi}} \ll I_{\mathrm{hc}}$).

2.3 Temperature dependence

The temperature dependence of the avalanche current is mainly due to the temperature dependence of b_n. We will use the same formulation as in [1]

$$b_n(T) = b_n(T_{\mathrm{ref}})\,(1+7.2\cdot10^{-4}\,\Delta T - 1.6\cdot10^{-6}\Delta T^2), \tag{17}$$

where ΔT is the device temperature minus the reference temperature $T_{\mathrm{ref}} = 300\mathrm{K}$.

3 Comparison with measurements

This avalanche model becomes part of a new release of the bipolar compact transistor model Mextram (release 504). A test version of Mextram 504 is built into our in-house circuit simulator. The simulations are performed with the full Mextram 504 model including self-heating of the device. The emitter dimension of the DUT is $0.6\times5.4\,\mu\mathrm{m}^2$ and the test structure contains five transistors in parallel. The measurements are performed at various base-emitter voltages ranging from 0.75–$1.05\,\mathrm{V}$. The base-collector voltage is swept from 0 to $14\,\mathrm{V}$. Two parameters (W_{epi} and N_{epi}) are extracted from the collector voltage dependency at small collector currents and the third (S_g) from the high current regime. The hot carrier current I_{hc} is also used in the avalanche model but extracted from the DC gain at small collector voltages where the avalanche current is zero. The extracted parameters are: $W_{\mathrm{epi}} = 1.10\,\mu\mathrm{m}$, $N_{\mathrm{epi}} = 2.82\cdot10^{15}\,\mathrm{cm}^{-3}$, $S_g = 0.55$ and $I_{\mathrm{hc}} = 2.24\,\mathrm{mA}$.

The measured and simulated base currents are shown in figure 4 and the collector currents in figure 5. The inverse of the gain I_b/I_c is plotted in figure 6.

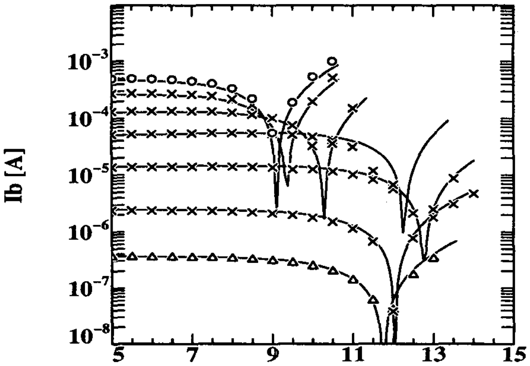

Figure 4: *Measured and simulated base current. Emitter dimension:* $0.6\times5.4\,\mu\mathrm{m}^2$*, 5 transistors in parallel for* $V_{\mathrm{be}} = 0.75, 1.05$*, with a step of* $= 50\mathrm{mV}$*. The extracted parameters are:* $W_{\mathrm{epi}} = 1.10\,\mu\mathrm{m}$, $N_{\mathrm{epi}} = 2.82\cdot10^{15}\,\mathrm{cm}^{-3}$, $S_g = 0.55$ *and* $I_{\mathrm{hc}} = 2.24\,\mathrm{mA}$.

During the measurement there is a significant increase of the device temperature due to self-heating. The thermal resistance of $232°\mathrm{C/W}$ is extracted from the increase of the collector current at high V_{be} and V_{bc}. For $V_{\mathrm{ce}} = 10\,\mathrm{V}$ and $I_c = 50\,\mathrm{mA}$ the temperature rise is already $116°\mathrm{C}$.

For characterization the collector voltage where the base current is zero is important, since it is the collector-emitter breakdown voltage BV_{ceo} with open base [4]. The

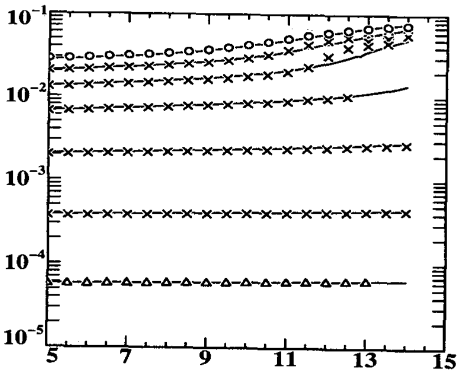

Figure 5: *Measured and simulated collector current. See fig. 4 for the measurement conditions and parameter values.*

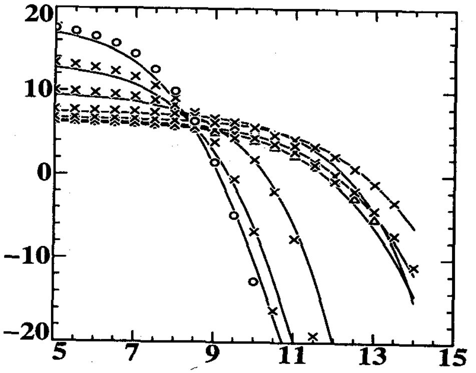

Figure 6: *Measured and simulated inverse gain I_b/I_c. See fig. 4 for the measurement conditions and parameter values.*

measured and simulated collector voltages where I_b is zero are plotted in figure 7. For lower currents the current modulation of the electric field causes E_m to decrease. To generate the same avalanche current (needed to make I_b zero) a higher collector voltage is needed. The maximum collector voltage is reached when the electric field in the space charge region becomes more or less flat and $E_0 \approx E_w$. Below the maximum the transistor is operating in the normal forward mode. Beyond the maximum the electric field E_0 at the junction decreases rapidly and the transistor goes into quasi-saturation. An injection layer with thickness x_i is formed and W_d decreases according to Eq. (12). This gives an additional increase of E_m and therefore of $I_{\rm avl}$. As a result the collector voltage where $I_b = 0$ decreases strongly with collector current. That the transistor is in quasi-saturation can also been seen in figure 6. The inverse gain I_b/I_c at $V_{\rm cb} = 5\,\rm V$ increases strongly, which means that the gain itself decreases. The calculated thickness of the injection layer according to the Mextram compact model is plotted in figure 7.

4 Summary

In this paper we derive a comprehensive avalanche multiplication model for circuit simulation. At small collector current levels the avalanche current is a function of the thickness and doping level of the epilayer. At high current levels the current spreading, doping profile of the buried layer and quasi-saturation are important to describe the maximum electric field. The maximum electric field, its distribution and self-heating are taken into account to calcalute $I_{\rm avl}$. The measured base and collector current are excellent modelled over a large range of base-emitter and base-collector voltages. This includes the description of the breakdown voltage $BV_{\rm ceo}$ and snap-back behavior [5].

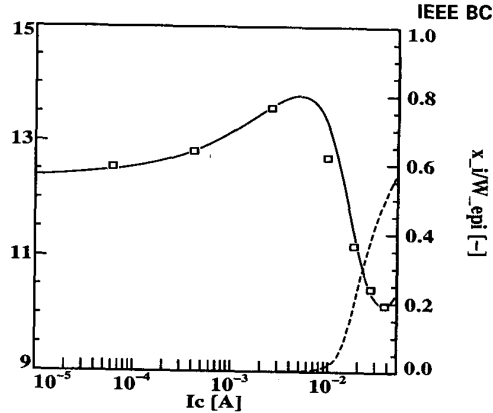

Figure 7: *Measured and simulated collector-emitter voltage when I_b is zero. This voltage is the collector-emitter breakdown voltage BV_{ceo} with open base. The dashed line gives the relative thickness of the injection layer according to the Mextram transistor model.*

For high speed BJT transistors with a very thin and highly doped epilayer the avalanche multipication, based on the local electric field distribution, will be overestimated [6]. Then this model will be no longer valid, but still reasonable accuracy can be obtained at the expense of the physical meaning of the extracted parameters.

This avalanche model becomes part of a new Mextram 504 release, but can be implemented also in other models.

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