An S-parameter Technique for Substrate Resistance Characterization of RF Bipolar Transistors

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ABSTRACT: An off-state s-parameter technique characterizes the NPN substrate resistance-capacitance network. The results are useful in designing RF test structures, modeling substrate effects for circuit simulation, and characterizing perimeter and area capacitance components from a single device.

I. Introduction

Components built in silicon processes invariably suffer from degradation in AC performance at high frequencies through power coupling to the substrate. Understanding and modeling this coupling is the key to minimizing losses. For NPN transistors, the Fmax benchmark parameter has been shown to exhibit a non-monotonic functional dependence on the total substrate resistance [1]. These authors correctly point out that maximum power transfer to the substrate occurs when the best match to the substrate port is realized. Fmax is at a minimum when power loss to the substrate is maximized. Substrate resistance (Rsub) estimates for their work were based on calculations rather than measurements.

Others have devised Rsub extraction techniques that are targeted for use in layout parasitic extraction applications [2]. These authors use an on-state Rsub measurement technique as verification of their work. On-state Rsub extraction techniques require a compact model that has already been optimized to the device under test. In addition, extensive work has been done developing specialized device simulation tools for analyzing substrate effects [3][4]. Those authors also suggest various lumped models for use in circuit simulators.

We present a substrate network extraction technique based on off-state s-parameter measurements. Verification is provided by measurements on test structures designed to provide a range of substrate resistances. These data show nice agreement with circuit simulations in which Rsub is included. Measurements show that both Rsub and the substrate capacitance (Ccs) will decrease with increasing frequency. Both simple theory and circuit simulations predict this effect. This roll-off characteristic can be exploited through parameter optimization to obtain values for the resistance and capacitance components in the substrate network. Extraction of area and perimeter Ccs components from a single device can be an advantage over techniques that require multiple devices.

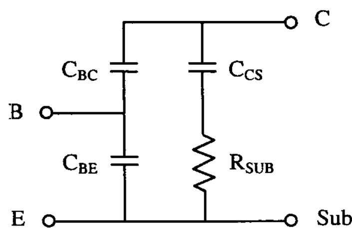

Figure 1. A simplified off-state NPN model in common emitter configuration used in deriving the substrate parameters.

II. Off-State Measurements

With Vbe = Vbc = Vcs = 0, the NPN transistor compact model reduces to a few capacitances and resistances. For NPN transistors built on high resistivity substrates, all other resistances are small compared to Rsub. This gives the equivalent off-state circuit as shown in figure 1. Then it is easy to derive the substrate resistance and capacitance.

$$Y_{22} = \frac{1}{R_{SUB} + \frac{1}{j\omega C_{CS}}} + j\omega C_{BC} \quad (1)$$

$$Y_{12} = -j\omega C_{BC} \quad (2)$$

$$R_{SUB} = \mathrm{Re}\left[\frac{1}{Y_{12} + Y_{22}}\right] \quad (3)$$

$$C_{CS} = \frac{-1}{\omega\, \mathrm{Im}\left[\frac{1}{Y_{12} + Y_{22}}\right]} \quad (4)$$

Test structures have been built in Philips Semiconductors' QUBiC3 RF technology [5]. A schematic cross-section for the QUBiC3 double-poly NPN is shown in figure 2. This process uses LOCOS and junction isolation. NPN transistors with an emitter area of 0.3×19.8 μm^2 were placed in RF characterization pads, each with different substrate tap spacing. The layout of the three taps used is shown in figure 3. Style 1 (0 µm) is a ring tap at minimum design rule spacing. Styles 2 and 3 have pairs of rectan-

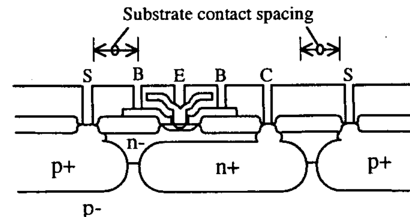

Figure 2. The Philips Semiconductors QUBiC3 double-poly NPN with substrate contacts shown.

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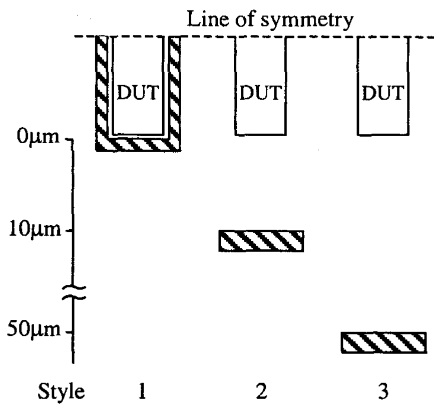

Figure 3. *Layout of three substrate taps used for silicon test structures.*

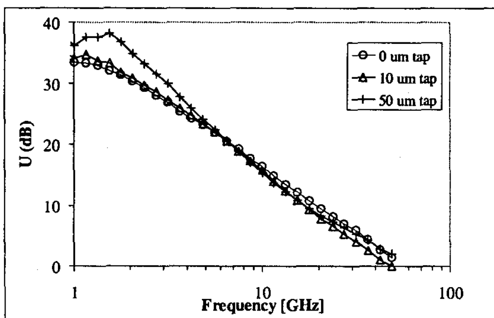

Figure 4. *Mason gain (U) measured for NPNs with different substrate tap spacing.*

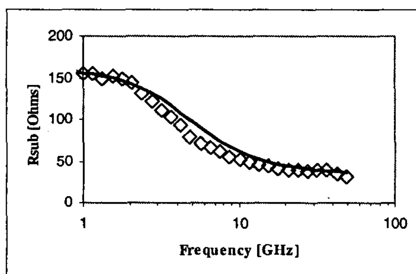

Figure 5. *Measured (symbols) and 9 lump model (line) Rsub over frequency for 0 μm tap structure in off-state.*

gular taps placed symmetrically 10 μm and 50 μm from the device, respectively. These structures were measured over frequency, in the on- and off-states, using a commercial on-wafer s-parameter characterization system. Careful open and short de-embedding was used for all measurements [6].

As expected fT showed no dependence on the different substrate resistances. The effect of substrate resistance on the Mason gain (U) is shown in figure 4. Note that U does not follow a single pole roll-off. The curve for the 10 μm tap shows the steepest slope of –22.9 dB/decade and hence the lowest Fmax. Extrapolation at –20 dB/decade on U measured at a fixed frequency can lead to erroneous values for Fmax.

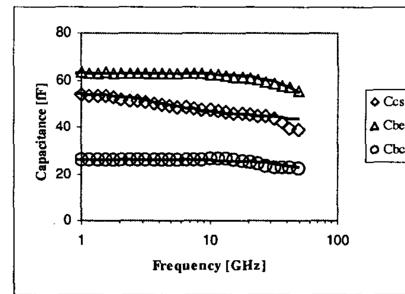

Figure 6. *Measured (symbols) and 9 lump model (lines) capacitances over frequency for 0 μm tap structure in off-state.*

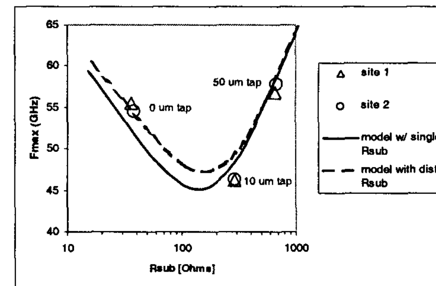

Figure 7. *Fmax plotted as a function of the extracted Rsub minimum. The solid line is the simulated Fmax vs. the model with a single Rsub. The dashed line is the simulated Fmax with a distributed Rsub. Rsub is extracted by the same off-state method for measured and simulated data.*

Rsub and Ccs were extracted from the off-state measurements using equations (3) and (4), respectively. The symbols in figures 5 and 6 show these results, as well as Cbe and Cbc from the off-state measurements. Observe that Rsub and Ccs decrease with frequency. This behavior is predicted by 1-D distributed capacitance theory and is the topic of the next section. Figure 7 shows the measured Fmax vs. the extracted minimum Rsub. This measured data is in good agreement with [1], which had Rsub values that were based on calculations.

The solid curve in figure 7 is from circuit simulation using the QUBiC3 library model with a single resistor added in series with the substrate connection. The standard NPN model in the QUBiC3 library is a geometry scalable Mextram model [7][8]. Mextram has been shown to model NPN high frequency behavior well over a range of bias conditions [9]. Note that Fmax is predicted quite well, even though the model parameters are optimized to fit fT and Rb from s-parameter measurements and Cbc from LCR measurements.

III. DISTRIBUTED SUBSTRATE NETWORK

In reality, Rsub is not a single lumped element, but is distributed across the bottom of the buried N^+ (BN) layer, as illustrated in figure 8. The total Rsub will also include the contribution of the exterior resistance to the substrate tap. Likewise, total Ccs will include both the distributed bottom capacitance and the perimeter capacitance. The BN layer of the NPN used in this study is approximately

21x5 μm². This high aspect ratio encourages us to consider a first model from 1-D distributed element theory.

A 1-D model of distributed capacitance and resistance in which the number of RC lumps goes to infinity gives

$$Zeff = Z_0 \coth(\gamma) \tag{5}$$

where $Z_0 = \sqrt{\frac{r}{j\omega c}}$ and $\gamma = \sqrt{j\omega rc}$.

These can be used to derive

$$\text{Reff} \cong \begin{cases} \frac{r}{3}, & \omega < \frac{9}{2rc} \\ \frac{r}{\sqrt{2rc\omega}}, & \omega > \frac{9}{2rc} \end{cases} \tag{6}$$

$$\text{Ceff} \cong \begin{cases} c, & \omega < \frac{2}{rc} \\ \frac{2c}{\sqrt{2rc\omega}}, & \omega > \frac{2}{rc} \end{cases} \tag{7}$$

where Reff and Ceff are the effective resistance and capacitance looking into the network; r and c are the total distributed bottom resistance and capacitance, respectively.

From the extracted Rsub and Ccs data shown in figures 5 and 6, one can compute the total distributed resistance for our test structure by using the corner frequencies given in equations (6) or (7). The value of $Rsub_{bottom}$ obtained is 32 kΩ. The corner frequency is easier to observe when the Rsub and Ccs data are plotted on a log scale.

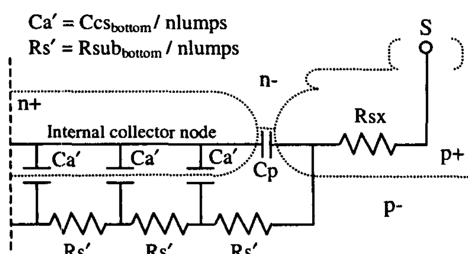

Figure 8. An expanded view of the substrate cross-section that shows the lumped model for the substrate network.

Another approach is to build a lumped circuit model of the type shown in figure 8, followed by parameter optimization to find values for all components. We have done this for the 0 μm tap structure, breaking up the distributed bottom capacitance into 9 R-C lumps. The capacitors are of course junction capacitors with voltage dependence. For the model to be correct for both on- and off-state simulations, junction capacitor models must be used. The off-state results are shown as the solid lines in figures 5 and 6. We also show (dashed line in figure 7) the result of simulating Fmax using the QUBiC3 library model with this lumped substrate model. The fit to the measured data is improved for low Rsub values.

The optimized values for the lumped model components are shown in table I. For comparison the values of the bottom and perimeter Ccs components from the library models are also shown. The library models were extracted from LCR measurements over many test structures with varying ratios of BN area to perimeter.

TABLE I.
Comparison of Parameter Sets (0 μM tap)

	Lumped model	Library
Ccs_{bottom} (fF)	11	11
$Ccs_{perimeter}$ (fF)	44	42
$Rsub_{bottom}$ (Ω)	8000	n.a.
Rsx (Ω)	32	n.a.

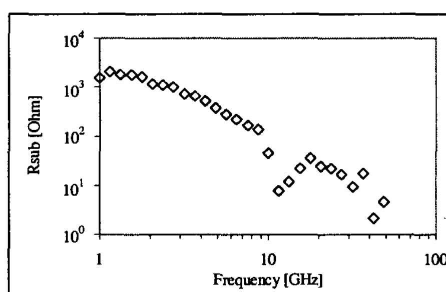

Figure 9. Measured Rsub over frequency for deep trench isolated QUBiC4 NPN.

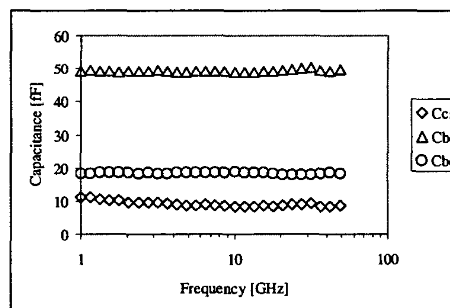

Figure 10. Measured capacitances over frequency for deep trench isolated QUBiC4 NPN

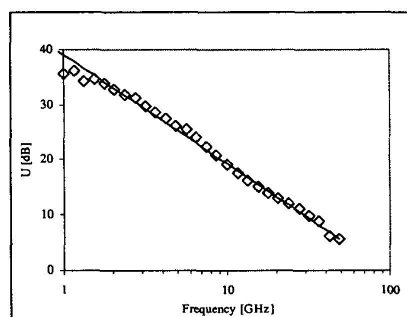

Figure 11. Measured Mason gain (U) for deep trench isolated QUBiC4 NPN.

The optimized value for $Rsub_{bottom}$ is a factor of four smaller than the value crudely obtained by the 1-D theory. We find that the presence of the perimeter capacitance does modify the roll-off characteristics. Nevertheless, the value from 1-D theory provides an adequate starting value for lumped model optimization. Observe that the optimized capacitances do agree quite well with the library values. Ccs can be difficult to measure accurately with an LCR meter because of its distributed nature and high series resistance. This s-parameter technique is stable and allows diagnostics on single devices.

IV. Deep Trench Isolation

QUBiC4 is the next generation of Philips Semiconductors' RF BiCMOS technology that is in development. The QUBiC4 NPN uses shallow and deep trench isolation to drastically reduce perimeter capacitances. The results of applying our off-state technique to a QUBiC4 transistor are shown in figures 9 and 10. The QUBiC4 device has roughly the same emitter size as the QUBiC3 device used in the other measurements. A low Ccs value is confirmed. And, reduction in Rsub and Ccs over frequency is still observed. Moreover, the reduction in Rsub is much greater than is measured on the QUBiC3 NPN. Figure 11 illustrates that the resulting change in coupling to the substrate reduces the slope of U to –19.9 dB/decade. For comparison, the slope of U measured on the QUBiC3 test structure (0 µm tap) is –21.2 dB/decade. The QUBiC4 device characteristics shown here do not necessarily represent the final process specifications.

Conclusions

Complex RF circuits increasingly put demands on device models. As applications in silicon move to higher frequencies, modeling of substrate effects becomes important.

The s-parameter technique presented here provides for a better understanding of the NPN substrate resistance network, and allows 1) optimization of test structures for more accurate device benchmarks, 2) extraction of substrate resistances for more accurate circuit simulation, and 3) characterization of Ccs bottom and perimeter components from single devices.

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