

## Explorations for High Performance SiGe-Heterojunction Bipolar Transistor Integration

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### Abstract

We present a SiGe HBT integration-study, introducing a low-complexity integration-scheme. We demonstrate a stepped box-like SiGe base-profile designed to reduce reverse Early effects, achieving  $f_T=55\text{GHz}$  and  $BV_{CEO}=2.7\text{V}$ . The transistor characteristics are well modeled by Mextram 504.

### Introduction

To succeed in the fast-growing and competitive SiGe playing field, a robust integration scheme and base design for the high performance SiGe-HBT is imperative.

For the integration, we propose a low-complexity non-selfaligned scheme including a composite etch-stop layer design for full RIE-damage protection of the SiGe-epi layer.

To obtain high performance SiGe-HBTs, our base is comprised of a boron spike embedded in a SiGe block *without* intentional grading.

For thorough assessment of both our SiGe-HBT performance and the new compact (SPICE) model Mextram 504 [1], we perform a full model parameter extraction.

Additionally, we simulate for the first time a measured modified reverse Early effect of the collector current and show how to circumvent it by base-profile optimization.

### SiGe-HBT Fabrication Process

Up to the base-epitaxy the presented integration scheme (Fig. 1) is identical to nearly any high-performance silicon bipolar transistor, starting with  $n^+$  buried layer formation and growth of a  $0.8\mu\text{m}$  thick collector-epi layer.

After formation of the shallow trenches and the collector sinker, a  $5 \cdot 10^{12}\text{cm}^{-2}$  280keV phosphorus collector implant is performed and the crystal damage is removed by a 10sec  $1030^\circ\text{C}$  rapid-thermal anneal.

We have opted for collector implant before SiGe-epi. This prevents the boron spike in the SiGe layer from degrading by transient-enhanced diffusion (TED) caused by the implant damage [2].

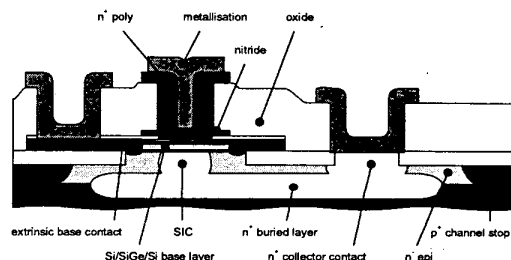


Figure 1: In the applied integration scheme (not drawn to scale) the SiGe-epi layer is protected from any RIE-damage.

Subsequently a thin wetting oxide layer is grown and a polysilicon layer is deposited, and removed again in the active areas. This layer is used to aid nucleation on the field and improve cleaning, as now almost the entire wafer is hydrophobic.

Immediately prior to loading the wafers into the ASM Epsilon-One reactor, the wafers are cleaned by standard FSI and 4 minutes in 1% HF. Prior to epitaxy, the wafers receive a hydrogen bake of 5 minutes at  $900^\circ\text{C}$  in the epi reactor chamber.

Subsequently, the base (Fig. 2) is grown in a blanket fashion, using a combined  $\text{SiH}_4/\text{SiH}_2\text{Cl}_2$ -process. The grown base consists of a 15nm 5% SiGe pedestal next to a 40nm 15% SiGe block. The stepped Ge-profile is grown without intentional grading. The 5nm

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$3 \cdot 10^{19} \text{cm}^{-3}$  boron spike is positioned 5nm inside the 15% Ge-block. We use a 30nm  $5 \cdot 10^{18} \text{B/cm}^{-3}$  p-type silicon capping layer.

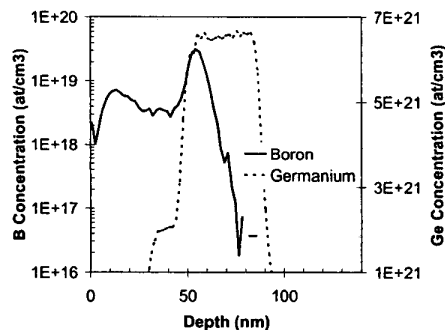


Figure 2: SIMS-profile (as-grown) of the SiGe-HBT base, which consists a stepped SiGe block containing a boron spike. No intentional Ge-grading has been applied. We use a p-type Si capping layer.

Following a passivation of the grown layer with a chemical oxide formed by a  $\text{HNO}_3$  wet-etch, an oxide/nitride layer stack is formed, which serves as an etch-stop layer during the emitter-opening etch[3].

The composite layer stack enables us to protect the strained mono-crystalline layer stack from any Reactive Ion Etching (RIE) damage. Exposure to plasma etching and subsequent annealing can cause relaxation of the strained SiGe layer [4].

We first plasma-etch the nitride, stopping in the extrinsic base on the underlying thin oxide layer, which subsequently serves as a screen oxide for the non-selfaligned base link implant. This implant also prevents the collector-base depletion zone to reach the defects around the poly-mono transition. Following resist strip, the implant is annealed, the extrinsic base polysilicon layer is patterned, and a thick oxide layer is deposited.

The emitter contact is established by using DUV-lithography, enabling device dimensions down to  $0.3 \mu\text{m}$  emitter width. We etch a window in the oxide selectively to the nitride. Subsequently, we reveal the active area by wet etching the remaining nitride and underlying oxide, thus preventing the generation of RIE damage to the intrinsic base.

We find that we have to place the emitter window at least 150nm away from the epi poly-mono transition region to prevent EB-shorts caused by the twin dislocations in this region [3].

Subsequently, an *in-situ*  $3 \cdot 10^{20} \text{cm}^{-3}$  arsenic doped polysilicon layer is deposited with no intentional interfacial oxide at the poly-mono interface using a vertical furnace with a loadlock. This enables epitaxial alignment of the polysilicon emitter [5].

We pattern the emitter polysilicon and perform a relatively low temperature emitter-RTA of  $1000^\circ\text{C}$  10sec, enabled by the insitu emitter-poly.

Finally, with the contact window etch and the formation of standard one-level Al-metallisation, the transistor is completed.

## Electrical Results

Fig. 3 shows a typical Gummel plot of a  $1.1 \times 10.1 \mu\text{m}^2$  transistor, demonstrating ideal  $I_C$  and  $I_B$  down to low base-emitter-bias. The drawn lines demonstrate the excellent modeling obtained by Mextram 504 simulations (see below).

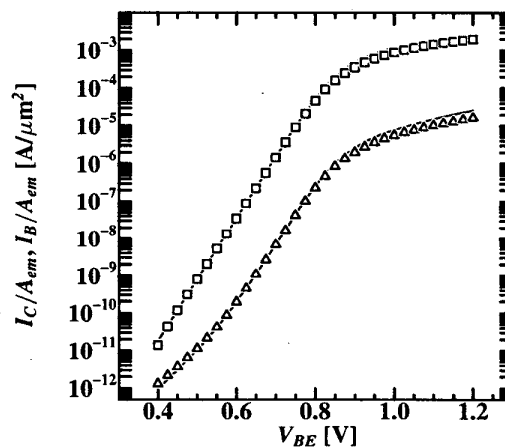


Figure 3: Gummel plot of a SiGe HBT with  $A_{em} = 1.1 \times 10.1 \mu\text{m}^2$ , showing ideal slopes for the base and collector current. The drawn lines show the Mextram 504 model simulations.

Due to the epitaxial alignment of the emitter poly, we can ensure a high surface-recombination velocity [5]. We consequently obtain a high base-current density and a relatively low current gain of about 225 (Fig. 4). As desired by designers, the current gain is nearly flat over several decades of  $I_C$ .

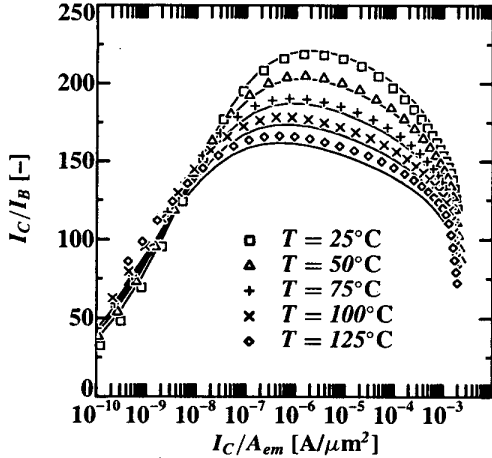


Figure 4: Temperature scaling of the current gain. The low  $h_{fe}$  is obtained by an epitaxially-aligned emitter. The drawn lines show the Mextram 504 model simulations.

The current gain also features a negative temperature coefficient. The parts of the transistor which are heating up, are thus drawing less power. This provides a negative feedback mechanism, contrary to the thermal runaway observed with conventional silicon bipolar transistors. This is especially desirable for large area power-transistor applications.

For practical reasons, the output characteristics in Fig. 5 are measured in the middle of the operating temperature regime at  $T=75^\circ\text{C}$ .

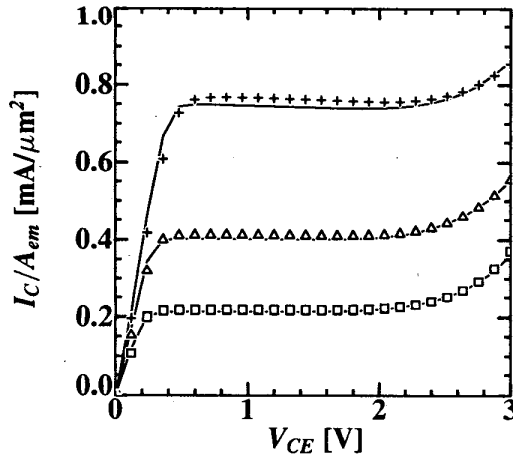


Figure 5: Output characteristics at  $T=75^\circ\text{C}$ .  $BV_{CEO}$  is 2.7V while  $V_A$  exceeds 150V. The drawn lines show the Mextram 504 model simulations.

The Early voltage is greater than 150V. We obtain a collector-emitter breakdown voltage of 2.7V, enabled by the low current gain of 225.

At high currents, the output characteristics show a decrease in  $I_C$  with higher  $V_{CE}$ . This selfheating effect

is caused by the negative temperature coefficient of the current gain.

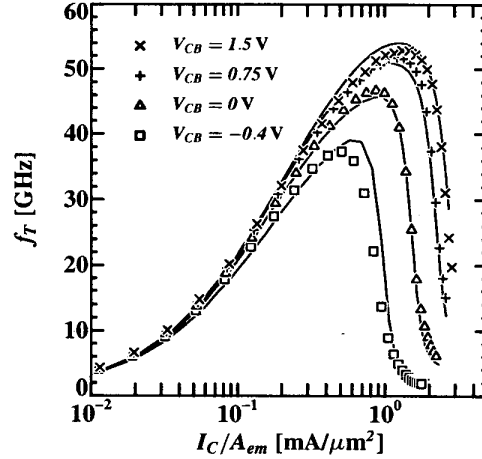


Figure 6:  $f_T$  as a function of the collector current. The peak  $f_T$  of 55GHz occurs at a collector current of  $2\text{mA}/\mu\text{m}^2$ . The drawn lines show the Mextram 504 model simulations.

Fig. 6 shows that we obtain with  $V_{CB}=1.5\text{V}$  a peak  $f_T$  of 55GHz at a collector current density of  $2\text{mA}/\mu\text{m}^2$ .

Table 1 gives a brief summary of the electrical results.

$f_T @ V_{BC}=1.5\text{V}$	55	GHz
$BV_{CEO}$	2.7	V
$V_A$	150	V
$h_{fe}$	220	-
$R_{pinch}$	8	$\text{k}\Omega/\square$
$BV_{EBO}$	3.0	V
$BV_{CBO}$	12.0	V
$C_{EB}$	7	$\text{fF}/\mu\text{m}^2$
$C_{CB}$	2	$\text{fF}/\mu\text{m}^2$

Table 1: Electrical results obtained on a SiGe-HBT at  $T=25^\circ\text{C}$  with  $A_{em}=1.1 \times 10^{-1} \mu\text{m}^2$ .

### Mextram 504 Modeling

We perform a full parameter extraction using the compact model Mextram 504 [1]. This serves as a test for the Mextram model and also increases the understanding of our SiGe-technology.

Our extraction includes measurements at five temperatures for obtaining temperature scaling, as shown in Fig. 4. This figure also demonstrates that Mextram 504 can model the reverse Early effect correctly. No additional non-ideality factor for the collector current had to be introduced in the model.

The output characteristics (Fig. 5) demonstrate that Mextram is also capable of modeling the forward

Early effect, avalanche multiplication and self-heating effects well.

Fig. 6 shows that the model simulation of  $f_T$  is correct even beyond peak  $f_T$ . This requires good modeling of the collector epilayer.

The ability to model our HBT accurately is critical for a fast utilization of the SiGe-technology by designers.

### Capping Layer Profile Design

The p-type capping layer in case of box-like SiGe profiles requires careful optimization. We suggest a capping layer on top of the SiGe-box which is depleted for *all* bias conditions. If the EB-depletion layer becomes smaller than this capping layer, parts of the neutral base-region will be outside the intended SiGe box and the base Gummel number  $G_B$  will strongly increase with emitter-base bias. This results in an strong reverse Early effect, i.e. non-ideal  $I_C$ .

When using a non-optimized capping layer, we found electrically that  $I_C$  can even show two distinct *ideal* parts in the Gummel plot (Fig. 7).

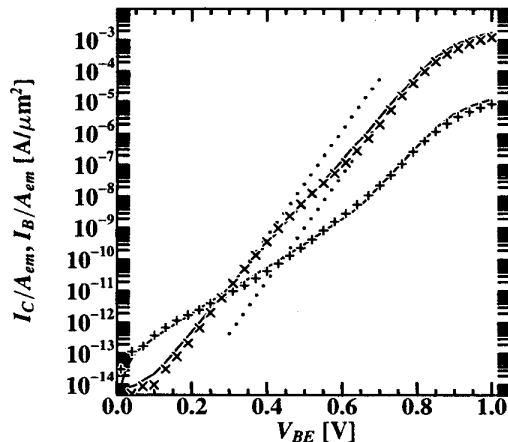


Figure 7: Measurement (xxxx) and corresponding device simulation (drawn-line) of a device with a non-ideal capping layer. We observe an enhanced reverse Early effect, which we relate in device simulations to the capping layer design.

We can explain this enhanced reverse Early effect in  $I_C$  by device simulations. In these we observe that in the ideal part of  $I_C$  at low  $V_{BE}$ , the EB depletion layer is relatively large and the neutral base is completely inside the SiGe box.  $G_B$  is determined by this box. At higher  $V_{BE}$ , however, the EB depletion layer is shrunk and the neutral base is partly in the capping layer and partly in the SiGe box.  $G_B$  is now mainly determined by the capping layer, which has a larger bandgap than the SiGe box.

A rule of thumb for the desired p-type capping layer thickness (after emitter diffusion) can be found from basic device physics equations;

$$W_{CAP} < \sqrt{\frac{2\epsilon_{Si}\epsilon_0 \cdot (V_{BI} - V_{BE})}{q \cdot N_{A,CAP}}}$$

where  $V_{BI}$  is the built-in voltage,  $N_{A,CAP}$  is the capping layer doping level and the other symbols have their usual meaning. In practice the internal  $V_{BI} - V_{BE}$  is limited to about 0.2V due to series resistance or high injection effects. For  $N_{A,CAP} = 3 \times 10^{18} \text{ cm}^{-3}$ , for instance, we suggest  $W_{CAP} < 10 \text{ nm}$ .

Adding some Ge to the capping layer reduces  $G_B$  outside of the Ge-block and therefore reduces the enhanced reverse Early effect. However, as the charge storage in the emitter-base depletion zone increases with the germanium percentage, we recommend a relatively low Ge-percentage for the pedestal region.

### Summary

We present a low-complexity integration scheme featuring STI, non-selective epitaxial growth, DUV-lithography and an epitaxially-aligned emitter to suppress the current gain. We protect, *both* in the intrinsic and extrinsic part of the transistor, the SiGe-epi from RIE-damage by using a composite layer stack as etch-stop.

We obtain  $f_T=55 \text{ GHz}$  with  $BV_{CEO}=2.7 \text{ V}$ ,  $R_{pinch}=8 \text{ k}\Omega/\square$  and  $V_A=150 \text{ V}$ . We present Mextram 504 model simulations showing an excellent agreement between modeled and measured device characteristics. Based on measurement and simulation results, we recommend a maximum thickness for the p-type capping layer to ensure good collector current idealities with SiGe-box profiles.

### Acknowledgements

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### References

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