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Statistical Characterization of 0.18μm Low-power CMOS Process using Efficient Parameter Extraction

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Abstract— **This paper illustrates the use of an efficient parameter extraction strategy for MOS Model 9 to perform a statistical analysis of sample devices from a 0.18μm CMOS process. The parameter extraction strategy allows all the parameters for a particular device geometry to be extracted from just 50 measurements. These parameters are subsequently used with Principal Component Analysis to provide best-case or worst-case model sets or as inputs to a Monte-Carlo experiment to investigate some of the performance trade-offs of the process.**

I. INTRODUCTION

An important factor influencing the yield of modern integrated circuits is the spread in device characteristics caused by the variability inherent in every manufacturing process. As power supply voltages are lowered to reduce power consumption and allow for mobile computing this process-induced variability does not scale downwards with the operating voltages and a reduced design window for circuit operation results. Thus, as supply voltages continue to decrease, it is ever more important to provide accurate characterization of the process variability and to account for this variability at the design stage to ensure the best possible product manufacturability. Traditionally, process variations have been characterized by standard end-of-line measurements including layer resistivities and first-order device characteristics such as threshold voltage and the low-field gain factor. While providing essential information for statistical process control these first-order parameters do not usually allow the variability of the parameters associated with sophisticated modern MOS models to be determined and provided to the design community. To characterize the parameter variability of sophisticated models it is helpful to perform parameter extraction as part of the end-of-line tests thus building up a large database of these parameters and allowing a meaningful statistical analysis to be performed. This paper presents the use of efficient parameter extraction techniques which are quick enough to be appended to the standard end-of-line measurements and applies these to devices from a 0.18μm process. The resulting parameters are used to select best-case and worst-case models for the leakage and maximum drive currents as well as to investigate the relationships between these quantities in a Monte-Carlo analysis.

II. THE PARAMETER EXTRACTION METHOD

The MOS model used for this work is MOS Model 9 (MM9). This public domain model provides accurate simulation for many process generations down to deep submicron dimensions and is suitable for digital, analogue and high frequency applications [1],[2]. The conventional approach to parameter extraction for this model is to measure a large set of I-V data from each region of device operation and then to optimize the model parameters with respect to this data in a pre-defined sequence. Depending on the device operating voltage, up to several hundred datapoints may be measured in this conventional approach and the resulting optimizations can take a minute or more of computer time. This conventional approach is too slow for volume data gathering purposes.

A more efficient extraction method based on the measurement of a greatly reduced dataset and analytical manipulation of the model equations has been proposed [3]. This method has previously been applied by the authors to 0.25μm CMOS devices for the purpose of statistical characterization [4]. In the present work the method has been further fine-tuned for 0.18μm CMOS technology with a lower operating voltage of 1.8V. This fine-tuning has involved a modification of the linear region extraction algorithms to include velocity saturation effects which have been seen to influence the linear region parameters for the very small device dimensions being considered. For a single device about 50 measurements are needed in total for the extraction of the full parameter set.

III. FIT QUALITY

Simulations using the MM9 parameters obtained with the efficient extraction method show excellent agreement with the measurements in all operating regions. Figure 1 shows the fit quality for the output characteristics of a device with a channel length of 0.18μm while figure 2 shows the corresponding fit to the output conductance. Figure 3 illustrates the fit quality in the subthreshold region. The quality of fit to other device dimensions is similar to that shown in figures 1 to 3. The extraction method also allows the substrate current parameters to be extracted but at the low operating voltage of 1.8V

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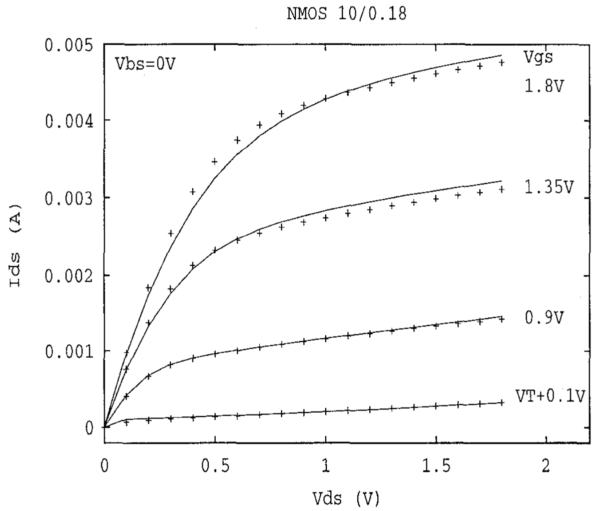

Fig. 1. Saturation region of an NMOS 10μm/0.18μm device. Symbols and lines represent measurements and simulations, respectively.

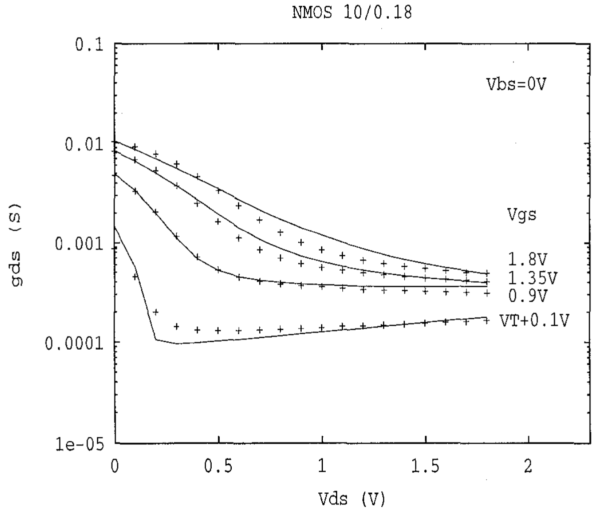

Fig. 2. Output conductance of an NMOS 10μm/0.18μm device. Symbols and lines represent measurements and simulations, respectively.

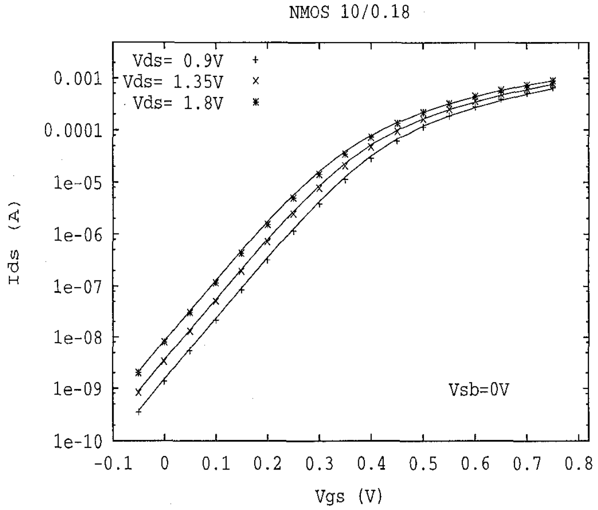

Fig. 3. Subthreshold region of an NMOS 10μm/0.18μm device. Symbols and lines represent measurements and simulations, respectively.

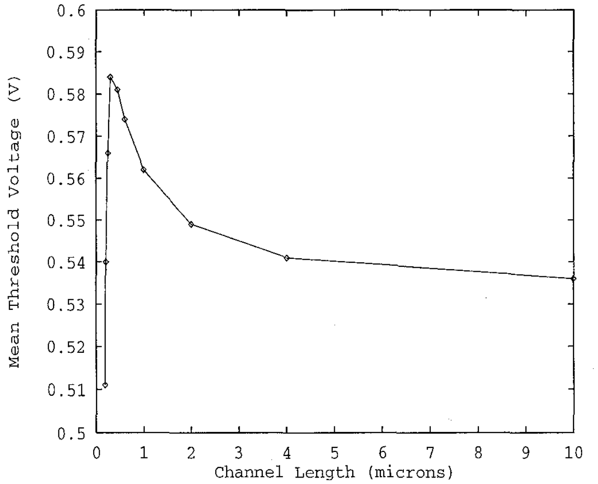

Fig. 4. MM9 threshold voltage as a function of channel length for the NMOS devices with a channel width of 10μm.

substrate current effects are negligible and are thus not illustrated here.

IV. APPLICATION TO VOLUME DATA GATHERING

MM9 parameter sets from a range of NMOS device geometries have been extracted from several sites on a test wafer from the 0.18μm process using the efficient extraction schemes. Figure 4 shows the variation of threshold voltage (the parameter VTO) with channel length for a constant width of 10μm - in this plot the mean value of VTO for a given channel length is shown. This figure illustrates that the conventional short channel effect occurs for gate lengths below 0.3μm while for lengths above this value a reverse short channel effect is apparent. Figure 5 shows the standard deviation of VTO as a function of channel length. It is seen that for channel lengths below about 0.4μm there is a large increase in the variability of the devices which has importance for the circuit operating window and analogue cell performance.

MOS Model 9 uses explicit scaling rules for many of the device parameters as a function of geometry and temperature. For instance, the geometrical scaling rule for threshold voltage (VTO) is shown in equation 1. Here W_E and L_E are the effective channel width and length respectively and can be obtained by plotting the low-field gain factor (BET) as a function of geometry. W_{ER} and L_{ER} are the effective dimensions of a reference device (this usually has a large width and a minimum-geometry gate length) and V_{TOR} is the threshold voltage of this reference device. $S_{W;V_{TO}}$ is the width scaling factor while

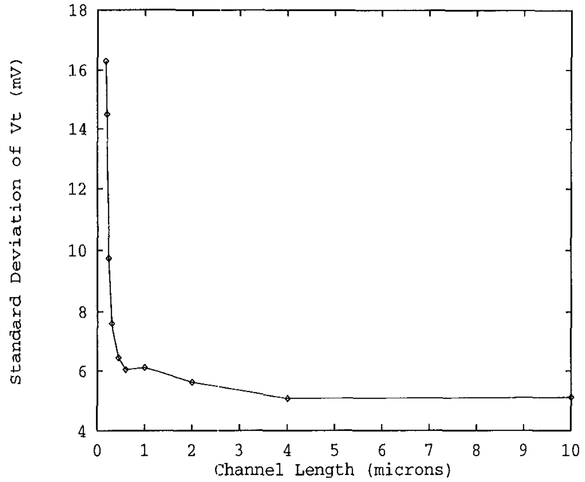

Fig. 5. Standard deviation of the threshold voltage as a function of channel length for the NMOS devices with a channel width of 10μm.

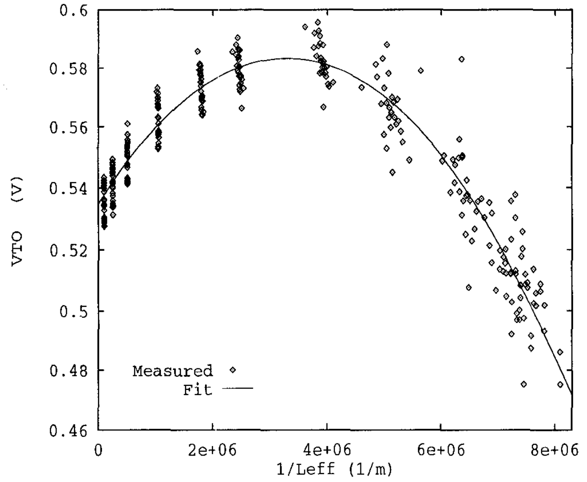

Fig. 6. MM9 threshold voltage as a function of effective channel length for the NMOS devices with a channel width of 10μm.

$S_{L;V_{TO}}$ and $S_{L2;V_{TO}}$ are the first and second order length sensitivities respectively.

$$\begin{aligned} V_{TO} &= V_{TOR} + \left(\frac{1}{L_E} - \frac{1}{L_{ER}}\right) S_{L;V_{TO}} \\ &+ \left(\frac{1}{L_E^2} - \frac{1}{L_{ER}^2}\right) S_{L2;V_{TO}} \\ &+ \left(\frac{1}{W_E} - \frac{1}{W_{ER}}\right) S_{W;V_{TO}} \qquad (1) \end{aligned}$$

Figure 6 shows the threshold voltage for approximately 250 NMOS devices ranging in gate length from 10μm to 0.18μm and having a constant channel width of 10μm plotted against the inverse of the effective channel length. The solid line shows a fit of the MM9 threshold voltage scaling rule to this data. It is apparent that the scaling rule accurately follows the observed length dependence.

V. STATISTICAL ANALYSIS

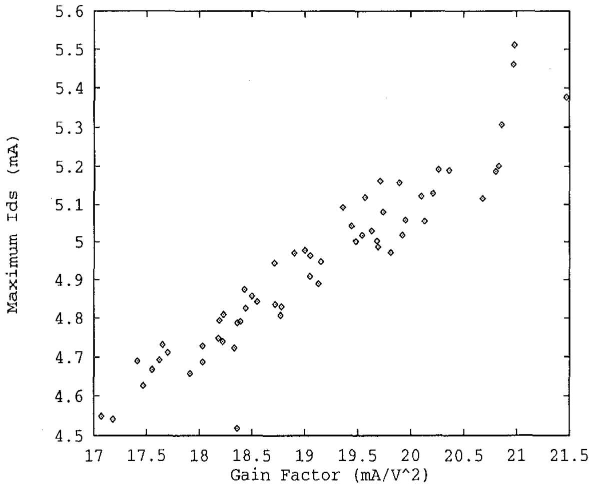

Fig. 7. I_{max} as a function of the MM9 gain factor for the NMOS 10μm/0.18μm devices.

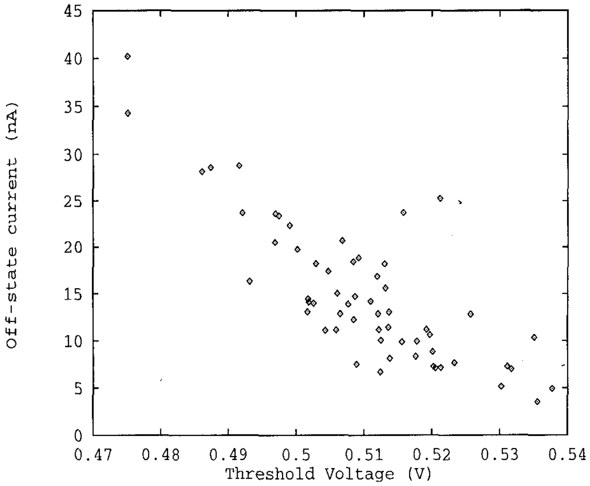

Fig. 8. I_{off} as a function of the MM9 threshold voltage for the NMOS 10μm/0.18μm devices.

In addition to the model parameters other device characteristics such as the maximum current and the leakage current have been measured. The maximum current (I_{max}) is defined as the drain current flowing under the conditions $V_{ds} = V_{gs} = 1.8V$, $V_{bs} = 0V$ while the leakage current (I_{off}) is measured for $V_{ds} = 1.8V$, $V_{gs} = V_{bs} = 0V$. The relationships between these quantities and the model parameters may then be investigated. Figure 7 shows the strong correlation which exists between I_{max} and the low-field gain factor for the short channel devices while figure 8 illustrates the relationship between the leakage current, I_{off}, and the device threshold voltage for the same geometry devices which shows a slightly less pronounced correlation than the previous figure.

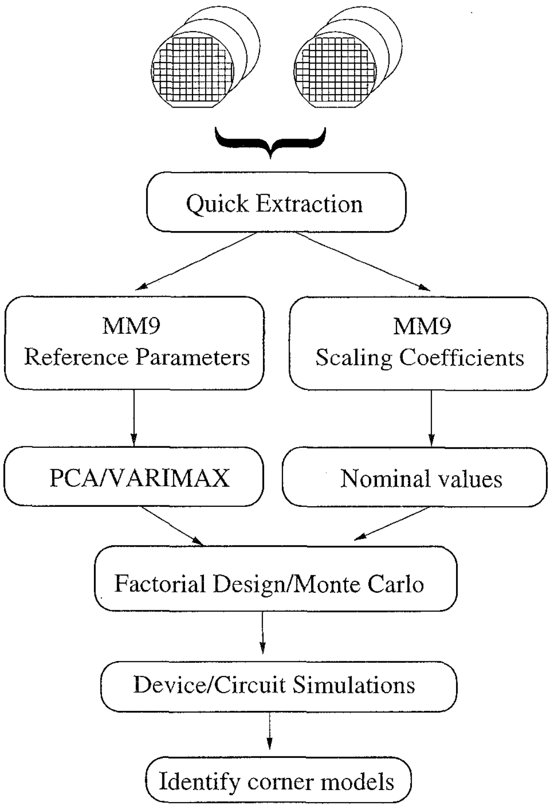

Fig. 9. Statistical methodology used for MM9 parameters.

Once parameter sets have been extracted for a large number of devices these can be analysed using statistical techniques such as Principal Component Analysis and VARIMAX rotations [5] to provide a reduced number of independent factors which can subsequently be used in the creation of best-case and worst-case models or for Monte-Carlo analysis. The statistical analysis approach used for MM9 is illustrated in figure 9. Following the treatment of [6] the model parameters representing the reference device and the scaling coefficients are treated separately. Either nominal or average values of the scaling coefficients are used while the reference parameters are analysed using PCA and a reduced number of principal components produced from these. These principal components are then used with the scaling coefficients in factorial or Monte-Carlo experiments to determine the corner models. To date, statistical analysis has only been performed for the device with dimensions $10\mu m/0.18\mu m$ from the $0.18\mu m$ process and so the scaling rules have not been used in the analysis that follows. It has been found that improved corner models can be obtained by using an experimental design formulation known as Box-Behnken as illustrated in figure 10 for the case of 3 independent factors - in this methodology not all independent factors are allowed to be at maximum or minimum values simultaneously.

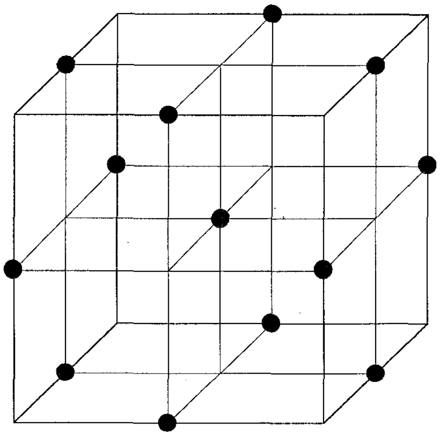

Fig. 10. 3 level Box-Behnken factorial design.

Figures 11 and 12 show the measured distributions of I_{max} and I_{off} respectively for sample NMOS $10\mu m/0.18\mu m$ devices. MM9 model sets were created by setting the principal components to $\pm 2.5\sigma$ around their mean values. The best-case and worst-case predictions for I_{max} and I_{off} resulting from these parameter sets are also indicated on the figures. It is seen that these predictions are in good agreement with the spread in the measured quantities. The results of using the principal components for a Monte-Carlo analysis is indicated by the bold lines on figures 11 and 12. Again it is seen that the Monte-Carlo results follow the measured characteristics closely - in particular the leakage current displays a tail at higher values which is matched by the Monte-Carlo simulations.

An important task for the design of low-voltage technology is to achieve the best possible trade-off between maximum drive current, I_{max}, and leakage current, I_{off}, and to account for the correlations between these two quantities during circuit design. Figure 13 shows the relationship between these two quantities from measurements of $10\mu m/0.18\mu m$ NMOS devices. Figure 14 shows the results of a Monte-Carlo analysis based on the Principal Components already obtained. It can be seen that the distributions and correlations of these two quantities predicted by the Monte-Carlo analysis closely match the measurements obtained. This illustrates that not only the spreads in the important characteristics but also the correlations can fully be accounted for in circuit simulation.

VI. CONCLUSIONS

An efficient parameter extraction method has been adapted and fine-tuned for low-power 0.18μm CMOS technology with a supply voltage of 1.8V. The method has been utilized to perform a statistical analysis of sample devices from this technology. This analysis demonstrates

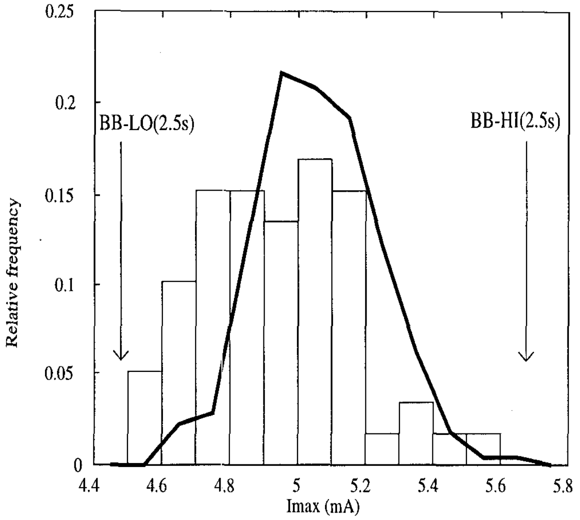

Fig. 11. Measured (histogram) and simulated (Monte-Carlo calculation using Principal Components) distribution of I_{max} for the NMOS 10μm/0.18μm devices. The Box-Behnken 2.5σ limits are also indicated.

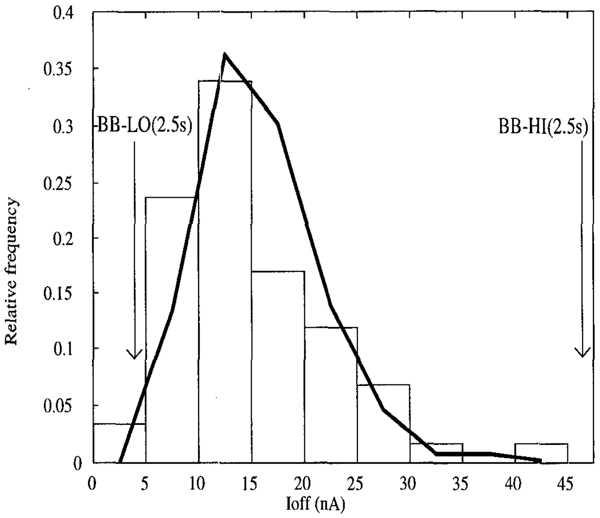

Fig. 12. Measured (histogram) and simulated (Monte-Carlo calculation using Principal Components) distribution of I_{off} for the NMOS 10μm/0.18μm devices. The Box-Behnken 2.5σ limits are also indicated.

that model parameter spreads and correlations can be taken into account during circuit simulation. The availability of this extraction method and simulation procedure in the early stages of process development is of use to investigate and improve the narrowing design window of modern CMOS technologies.

VII. ACKNOWLEDGEMENTS

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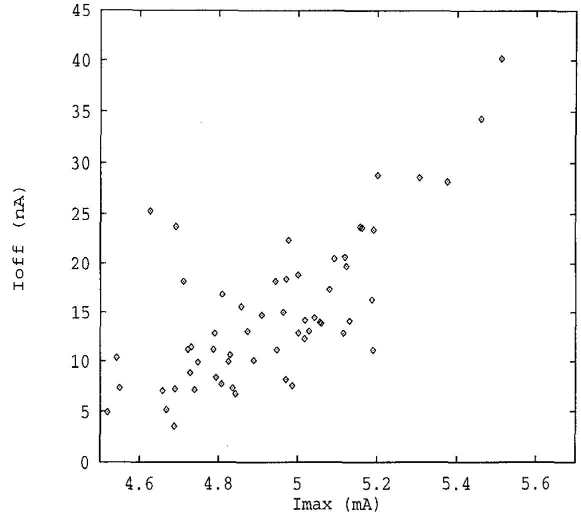

Fig. 13. Measured values of I_{off} versus I_{max} for the NMOS 10μm/0.18μm devices.

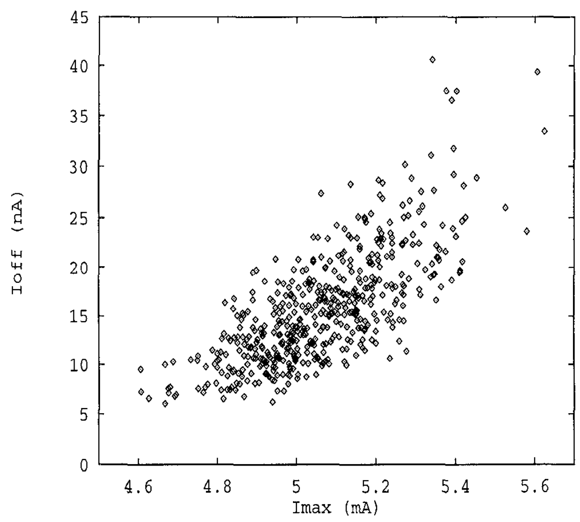

Fig. 14. Monte-Carlo simulations of I_{off} versus I_{max} for the NMOS 10μm/0.18μm devices.

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